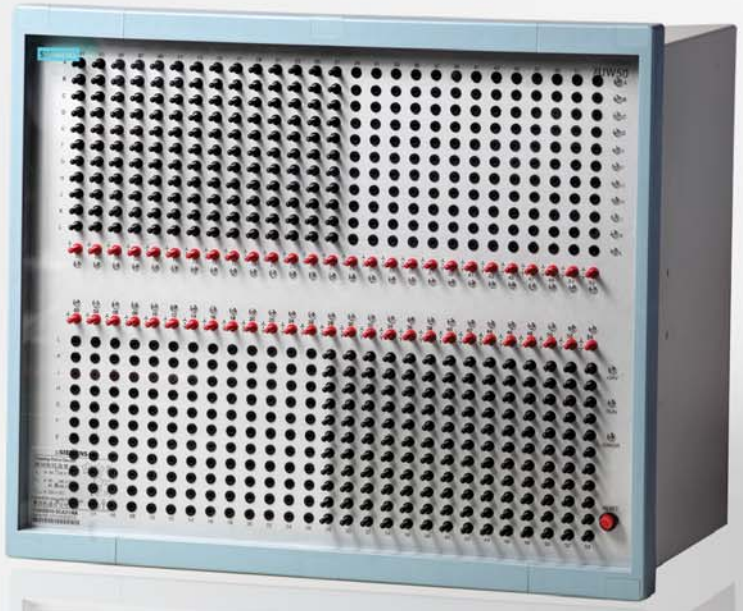


Tripping Matrix Device 7UW5010

As of Tripping Circuit Management Unit or
Non-electric Protection Device

Catalog 1.2

Answers for energy management.

SIEMENS

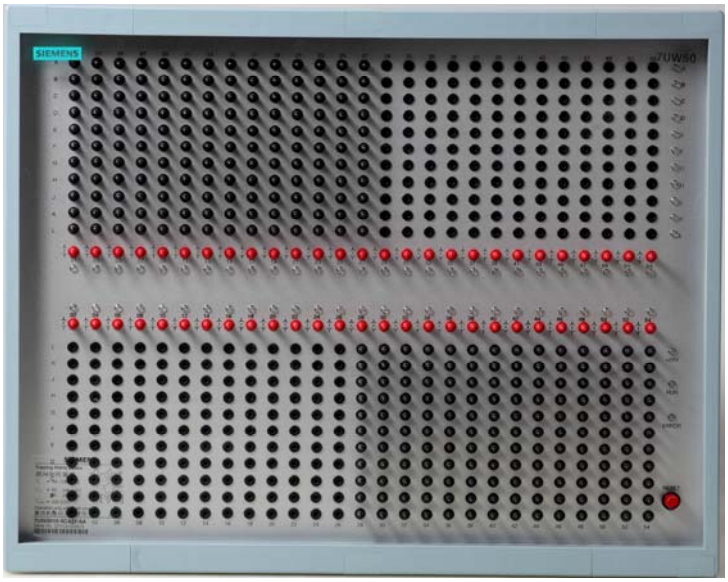


Fig.1 Front illustration of Tripping Matrix Device 7UW5010

APPLICATION 1
TRIPPING CIRCUIT MANAGEMENT UNIT

The tripping matrix device 7UW50 is a component of Siemens numerical generator protection system. The biggest advantage of the hardware tripping matrix module is to provide a transparent, visible, simplified and easily programmable facility for the combination of protection functions and output commands to variable tripping objects.

The tripping matrix device 7UW50 is developed to manage the tripping circuit of generator protection system for large power station block. With the integrated matrix module, the tripping scheme can be freely modified with the most flexibility to fit for different field requirements, i.e, the tripping objects of the protection function can be easily changed on site via the operation of logic plugs to assigned column on front panel.

The device 7UW50 is integrated with signaling modules for all matrix inputs from various protection units. Each input can be indicated by signaling relay with at least 3 potential-free contacts which can be routed for alarming to DCS, FR, RTU, etc.

The device 7UW50 is also, for all matrix outputs to different tripping objects, integrated with tripping modules. Each tripping relay has at least 2 potential-free contacts which can be routed for tripping to GCB, Field CB, HVCB, etc.

For local alarming purpose, latched LEDs are installed to indicate all matrix inputs and outputs. They can be locally reset via front RESET button or remote reset via binary input.

The integrated CPU module can help to record the status of matrix module. Any new information can be accessed locally via PC or sent to remote control centre via the serial protocol IEC 60870-5-103 or Modbus RTU over the electrical RS485 interface.

APPLICATION 2
NON-ELECTRIC PROTECTION DEVICE

Based on the above functionalities, the tripping matrix device 7UW50 can be used as the non-electric protection device too if no CFC function is required..

The non-electric tripping commands (e.g, from Heavy Buchholz relay) can be directly connected to the inputs of matrix module. After the matrix programming, the assigned outputs will initiate the tripping relays which are routed to respective tripping circuits. Note that the tripping behavior is immune to any transient disturbance due to the heavy initial power consumption (approx. 8.2W).

DESIGN and CONSTRUCTION

Modules inside the device:

- Matrix module
- Signaling module
- Tripping module
- Power module
- CPU and communication module
- LED indicating module

Matrix Module

The matrix module comprises input module and output module. Inputs (column) and outputs (row) are reliably connected via diode connectors (logic plugs). The inputs are equally divided into two groups. Both groups are arranged one over the other (see Fig.2) and electrically connected internally. To cater for the different requirements and applications, the matrix is equipped with 4 types, i.e, 54x11 (see Fig. 3), 30x11 (see Fig. 4), 54x2 (see Fig. 5 left) and 30x2 (see Fig. 5 right). That is, e.g, matrix module 54x11 has 54-input (each group with 27) and 11-output.

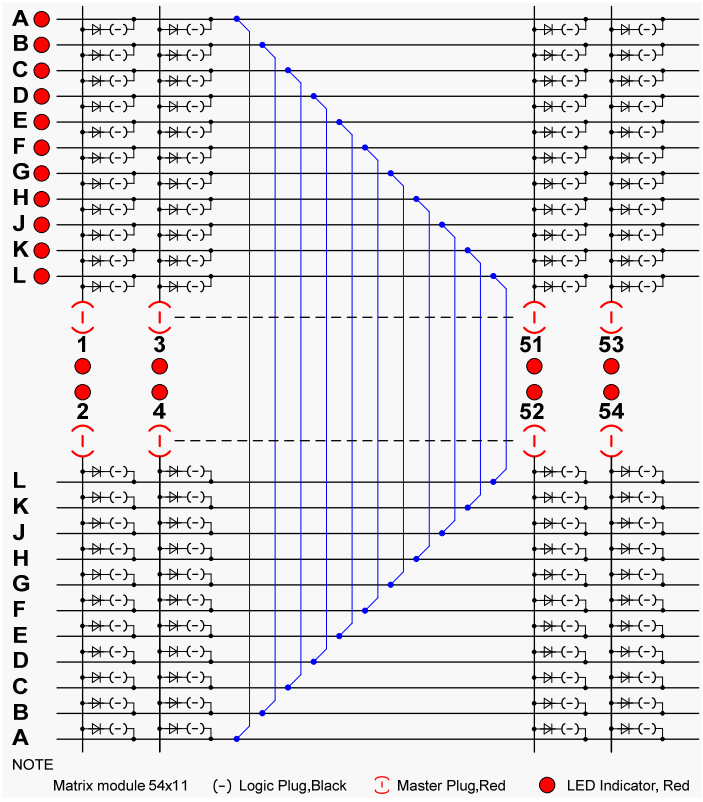


Fig.3 Diagram of matrix module 54x11

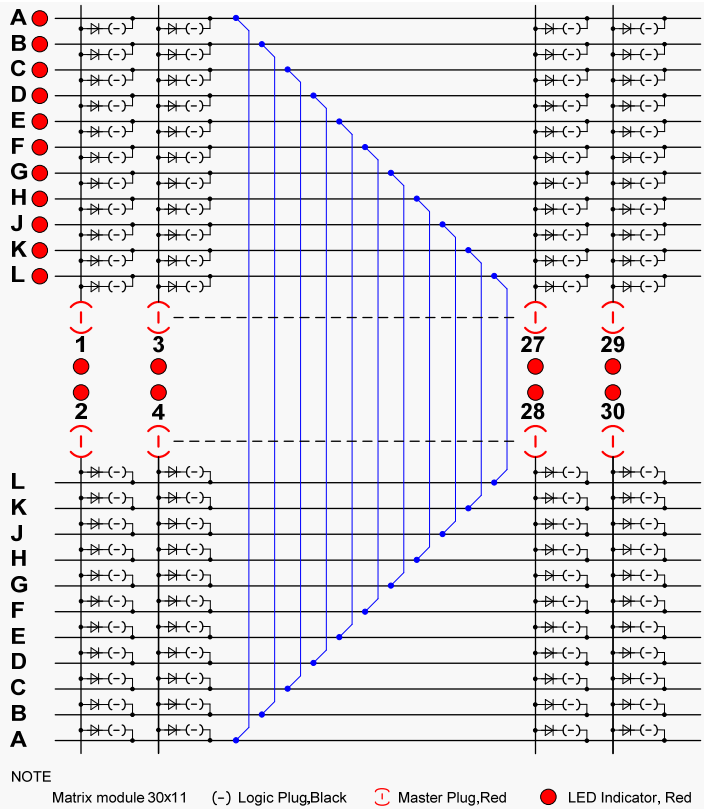


Fig.4 Diagram of matrix module 30x11

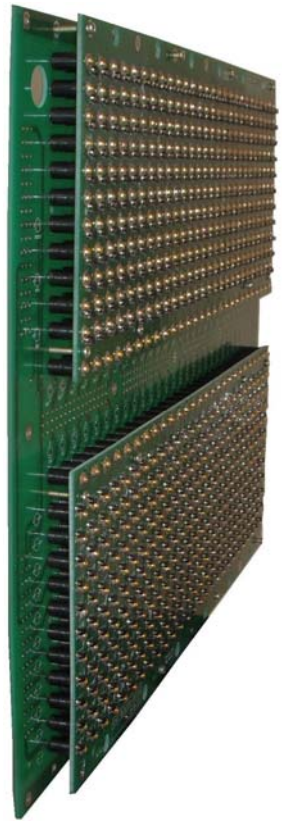


Fig.2 Matrix Module

Types of 54x11 and 30x11 are in principle designed to serve for tripping circuit management while 54x2 and 30x2 for non-electric protection. It could be mixed in some case.

Signaling Module

Each signaling module is designed for 6 matrix inputs, that means up to 9 signaling modules are required for the maximum 54 inputs. Every input is indicated by two grouping contacts and one individual contact. Even, the 1st and 3rd signaling relays on each signaling module separately have one additional individual contact.

The 1st and/or 4th signaling relay contacts with type of latching are optional. In this case, the module INL (MLFB position 9th= *B*) should be selected. Note that the 2nd and 3rd contacts for each input have been exclusively designed to be un-latched even in this case. All contacts are potential free.

Tripping Module

Each tripping module is designed for 6 matrix outputs, that means up to 2 tripping modules are required for the maximum 11 outputs. Each output is interpreted by two individual contacts.

Even, the 1st and 2nd tripping relays on each tripping module separately have two additional individual contacts.

Tripping module with type of lockout relay is optional. In this case, the module TRL (MLFB position 11th= *2* or *4*) should be selected. Note that the 5th tripping relay on each tripping module have been exclusively designed to be with un-lockout relays even in this case.

The contact form of tripping relay can be *all in Normal Open (NO) type* or *some in Normal Close (NC) type* which are respectively defined by ordering code (MLFB position 12th= *1* or *2*). All contacts are potential free.

External tripping relays can also be used if one of tripping modules is equipped without tripping relays (see Fig.21). In this case, the module OUT (MLFB position 11= 0, 3 or 4) should be selected.

CPU and Communication Module

CPU module is to take over the task of internal SOE and communication. The status of matrix module will be monitored and recorded. The messages can be locally accessed via Port C over PC, or remotely accessed by two control centers via two RS485 Ports of B1 and B2 over protocol IEC 60870-5-103 or Modbus RTU. The two ports can be individually set even with different protocols.

IRIG-B is implemented for time synchronization via Port A.

The specially designed software GPAcom is to serve for parameter setting of communication ports, time synchronization and local access to the device.

LED Indicating Module

Overall local alarming on the status of matrix module, power module and CPU module is done by LED indicating module. Latched LEDs is used for indicating the matrix module.

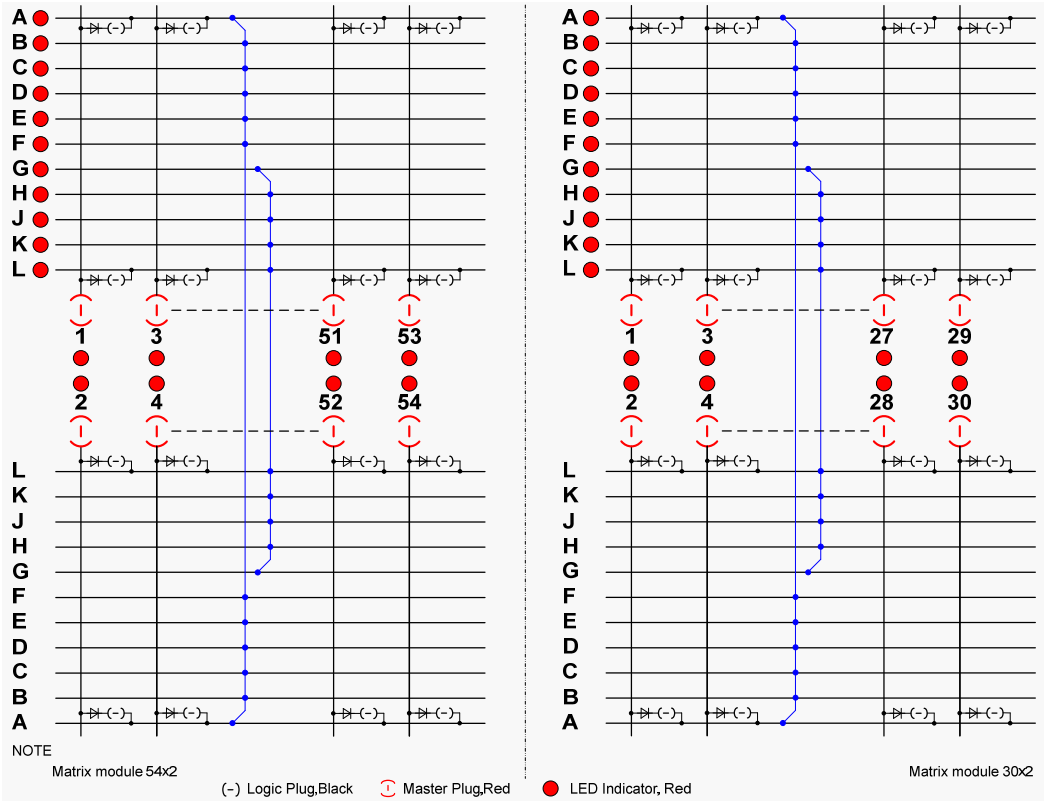


Fig.5 Diagram of matrix module 54x2 and 30x2

Power Module

LEDs and CPU are supplied by power module. Note that the signaling module and tripping module are directly powered by station's control voltage. That is to say, these modules can properly work even if the internal power module failed.

Module's Interaction

The interaction diagram among the matrix module, signaling module and tripping module is schematically shown in Fig. 6. Note that beside the remote signals, the LED indicators and SOE

are also initiated by signaling relays. The similar situation applies to tripping module.

To be noted that CPU module has no influence to modules of matrix, signaling and tripping.

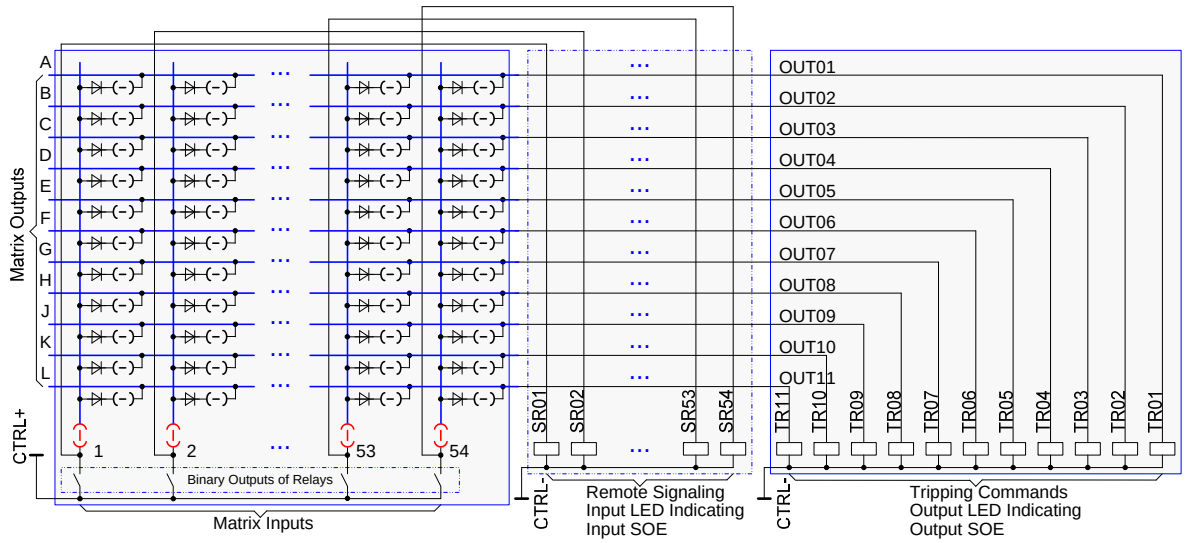


Fig.6 Schematic interaction diagram among modules of matrix, signaling and tripping

Plexiglass Front Cover

An additional plexiglass front cover protects the device against the dust invasion and unauthorized operation.

OPERATION

Connection between the protection functions and matrix module is implemented via master plugs (red), while the connection between matrix input and output via logic plugs (black). The plugs are plugged into the front panel of the matrix after the plexiglass front cover is removed.

A reset button is used for resetting all memories. This can be directly done on the plexiglass front cover. The memories (LEDs) can also be remotely reset via a binary input.

TRIPPING CONCEPT FOR NUMERICAL PROTECTION

Siemens SIPROTEC numerical protection units used for generator-transformer block incorporate an integrated software matrix. The required tripping objects by one protection function can be directly programmed over software DIGSI. If several multifunctional units are used for the protection system, the tripping contacts of the individual relays to the same tripping object must be connected in parallel (see Fig. 7). This is the tripping concept with software matrix.

If master tripping relays are inserted between the binary outputs integrated in the protection units and the tripping objects, the tripping combination can also be externally implemented. The master tripping relays then take over the task of decoupling the signals, multiplying the contacts of the integrated binary outputs and realizing the tripping combinations via the assignation of tripping signals (GCB, Field CB, ...) to form tripping commands from protection functions. Therefore, the binary outputs of the individual relays with the same required tripping consequence must be connected in parallel to activate the same mater tripping relay, and the contacts with the same tripping objects of various master relays must be externally connected in parallel to the respective tripping circuit (see Fig. 8). This is the tripping concept with master tripping relays.

If a variable arrangement of the tripping combinations is required for large generator unit, the hardware matrix described here can be very helpful. The binary outputs of protection functions from several protection units are to be directly routed to the inputs (rows in Fig. 9) of hardware matrix, meanwhile the tripping relays to the outputs (columns in Fig. 9). The operating contact of tripping relay is to be connected to the respective tripping circuit. This is the tripping concept with hardware matrix. The easy, fast and flexible combination of inputs and outputs on front panel of the device is visibly executed by the diode logic plugs. Note that at most 11 tripping objects can be connected regarding the matrix output up-limit.

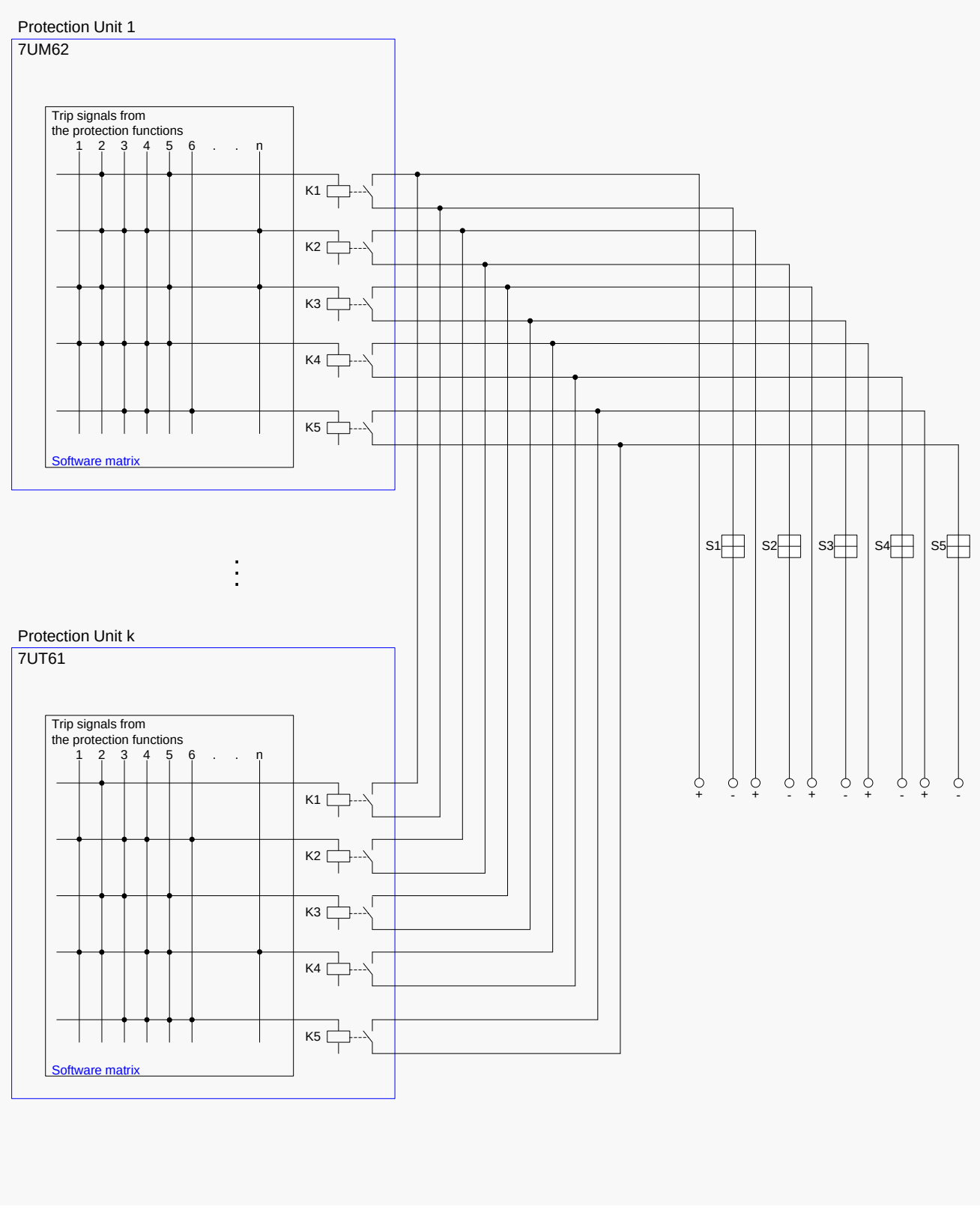


Fig.7 Tripping concept with software matrix

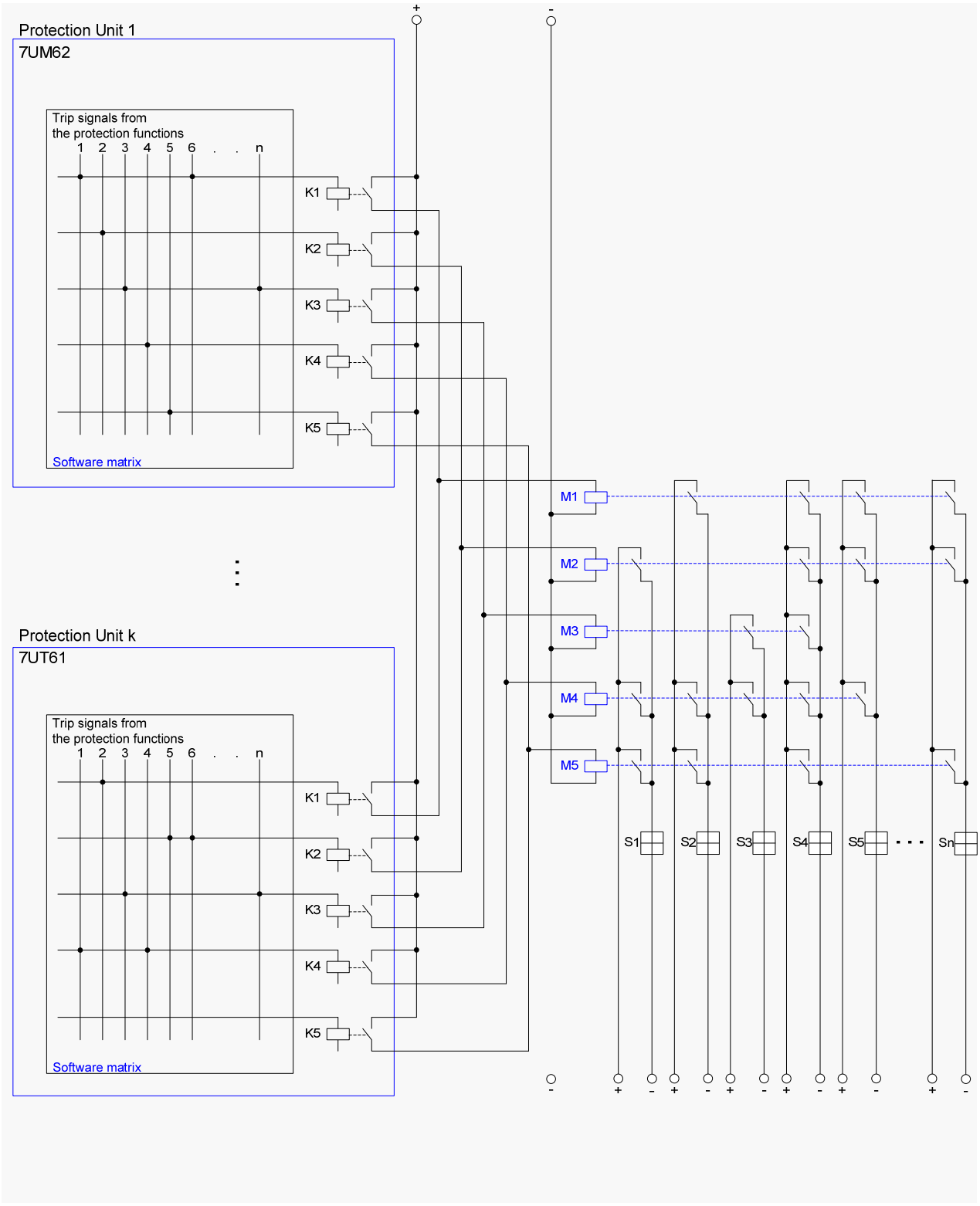


Fig.8 Tripping concept with master tripping relay

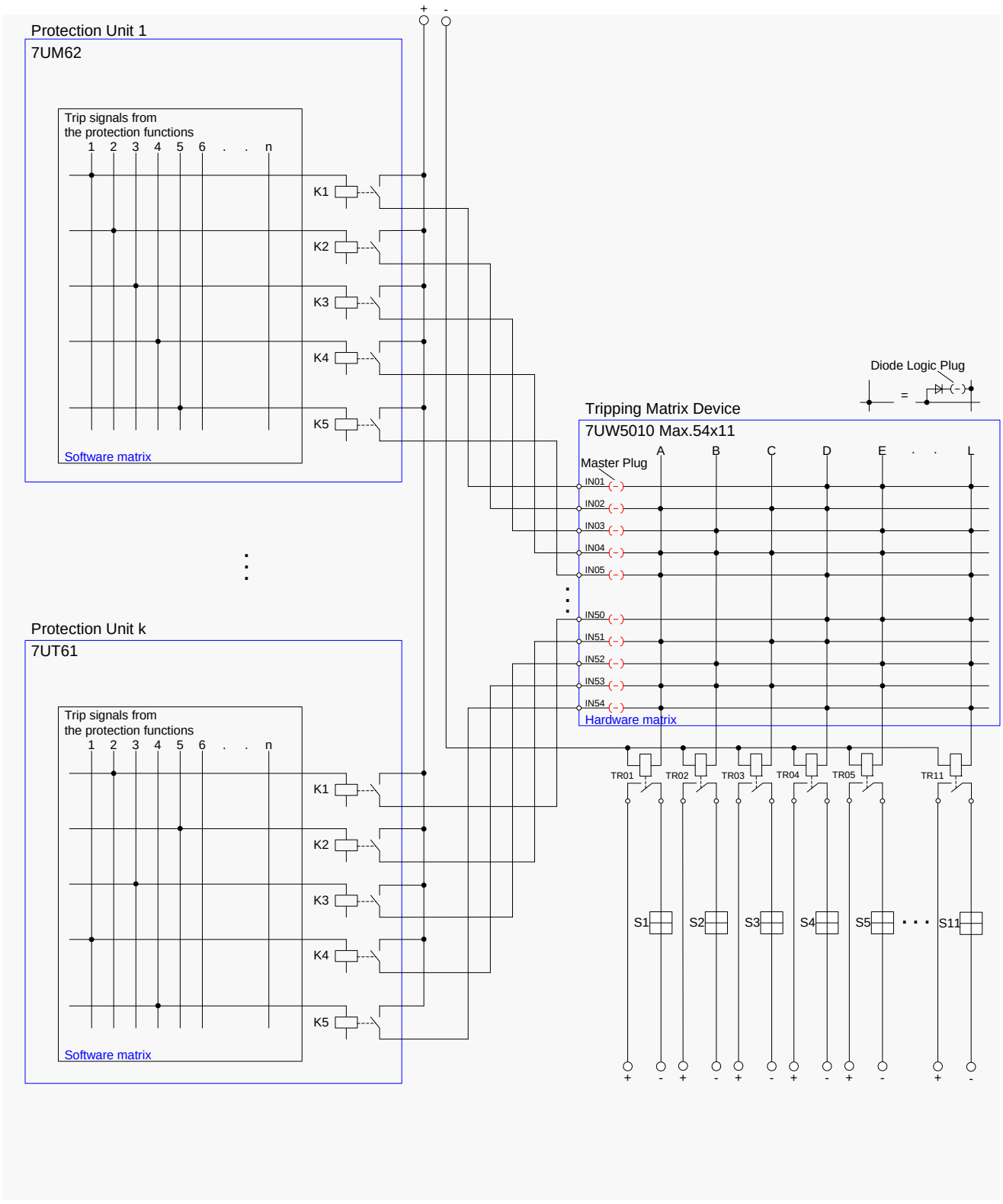


Fig.9 Tripping concept with hardware matrix

TECHNICAL DATA

Matrix Module	Matrix Type	54x11 30x11 54x2 30x2
	Number of columns (valid inputs)	54 30 54 30
	Number of rows (valid outputs)	11 11 2 2
Auxiliary Voltage	Rated control voltage U_{CTRL}	110V DC or 220V DC
	Auxiliary voltage range U_H	85-245V AC/DC
	Power consumption (approx.)	54x11 30x11 54x2 30x2
	quiescent ,in W	3 3 3 3
	energized (typical), in W	60 60 60 60
	Bridging time on auxiliary voltage failure	≥ 50 ms with UH ≥ 110 V
Diode Logic Plug and Master Plug	Maximum permissible current	Plug Diode 20A 1A
	Plug pin diameter	2.0mm
	Diode blocking voltage	1,000V
	Current flow direction	from column (+) to row (–)
	Scope of delivery	54x11 30x11 54x2 30x2
	Master Plug Pin, Red , in pcs.	54 30 54 30
	Logic Plug Pin, Black, in pcs.	330 176 108 60
Tripping Relays	Quantity of NO contact of each relay	
	if MLFB Position 12th = 1	TR01,TR02,TR07,TR08: 4 in individual TR03-TR06,TR09-TR11: 2 in individual
	if MLFB Position 12th = 2	TR01,TR07: 4 in individual TR02,TR05,TR08,TR11: 2 in individual TR03,TR04,TR06,TR09,TR10: 1 in individual
	Quantity of NC contact of each relay	
	if MLFB Position 12th = 2	TR02,TR08: 2 in individual TR03,TR04,TR06,TR09,TR10: 1 in individual
	Pick up voltage	55-70%Un
	Switching capacity	
	make	1,000W/VA
	break	30VA 40W resistive
	Switching voltage	25W/VA with L/R ≤ 50ms
	Permissible current	250V
	Operating time (Un, at 25°C/77°F), approx.	5A continuous
	non-Lockout type	8ms (excluding contact bounce time)
	Lockout type	10ms (excluding contact bounce time)
Signaling Relays	Quantity of NO contact of each relay	SR01,SR03,SR07,SR09,SR13,SR15,SR19,SR21 SR25,SR27,SR31,SR33,SR37,SR39,SR43,SR45 SR49,SR51: 4 (2 in individual, 2 in group) SR02,SR04-SR06,SR08,SR10-SR12,SR14, SR16 -SR18,SR20,SR22-SR24,SR26,SR28-SR30,SR32, SR34-SR36,SR38,SR40-SR42,SR44,SR46-SR48, SR50,SR52-SR54: 3 (1 in individual, 2 in group)
	Pick up voltage	55-70%Un
	Switching voltage	250V

	Permissible total current Operating time (Un, at 25°C/77°F), approx.	5A continuous 10ms
Alarming Relays	Life status Internal +24V DC monitoring	1 NO contact 1 NC contact
LEDs	Quantity RUN (Green) ERROR (Red) +24V DC (Green) Inputs (Red) Outputs (Red)	 1 1 1 54 11
Unit Design	Weight, approx. in kg Degree of protection acc. to IEC 60529 Housing Terminals	54x11 30x11 54x2 30x2 22.5 19 19.5 16 IP51 IP21
Serial Interfaces	Time synchronization (Port A) System Interface (Port B1/B2) Operator Interface (Port C)	IRIG-B, DC 5V 9-Pin subminiature connector (SUB-D) IEC 60870-5-103, Modbus RTU RS 485, 9-Pin subminiature connector (SUB-D) baud rate at 9,600/19,200/57,600/115,200 max. transmission distance at 1,000m RS 232, 9-Pin subminiature connector (SUB-D) max. transmission distance at 15m
Electrical Tests	Insulation Test Standard - High voltage test(routine test) all circuits except power supply, binary inputs and communication/time synchronization interfaces - High voltage test(routine test) power supply, binary inputs - High voltage test(routine test) only isolated communication/time synchronization interfaces - Impulse voltage test(type test) all circuits except communication/time synchronization interfaces, class III	 IEC 60255-5 2.5kV (rms), 50Hz DC 3.5kV 500V (rms), 50Hz 5kV(peak), 1.2/50µs, 0.5J, 3 positive and 3 negative impulses in interval of 5s.
	EMC Test for Immunity(type test) Standards - High frequency test IEC 60255-22-1, Class III - Electrostatic discharge IEC 60255-22-2, Class IV and IEC 61000-4-2, Class IV	 IEC 60255-6 and -22(product standards) EN 61000-5-2(generic standard) 2.5 kV (peak); 1 MHz; τ = 15 µs; 400 surges per s; test duration 2 s; Ri = 200 Ω 8 kV contact discharge; 15 kV air discharge; both polarities; 150 pF; Ri = 330 Ω

	- Irradiation with HF field, frequency sweep IEC 60255-22-3; Class III IEC 61000-4-3, Class III	10 V/m; 80 MHz to 1000 MHz; 10 V/m; 800 MHz to 960 MHz; 20 V/m; 1.4 GHz to 2.0 GHz; 80 % AM; 1 kHz
	- Irradiation with HF field, single frequency IEC 60255-22-3 and IEC 61000-4-3 amplitude modulated pulse modulated	Class III: 10 V/m 80/160/450/900 MHz; 80 % AM; duty cycle >10 s 900 MHz; 50 % PM, repetition frequency 200 Hz
	- Fast transient disturbance/burst IEC 60255-22-4 and IEC 61000-4-4, Class IV	4 kV; 5/50 ns; 5 kHz; burst length = 15 ms; repetition rate 300 ms; both polarities; Ri = 50 Ω; test duration 1 min
	- High energy surge voltages (SURGE), IEC 61000-4-5 Installation Class III auxiliary voltage Binary inputs and relay outputs	 impulse: 1.2/50 µs common mode: 2 kV; 12 Ω; 9 µF diff. mode:1 kV; 2 Ω; 18 µF common mode: 2 kV; 42Ω; 0. 5 µF diff. mode: 1 kV; 42Ω; 0. 5 µF
	- Line conducted HF, amplitude modulated IEC 61000-4-6, Class III	10 V; 150 kHz to 80 MHz: 80 % AM; 1 kHz
	- Power system frequency magnetic field IEC 61000-4-8, Class IV IEC 60255-6	30 A/m continuous; 300 A/m for 3 s; 50 Hz 0.5 mT; 50 Hz
	-Oscillatory surge withstand capability IEEE Std C37.90.1	2.5 kV (peak value); 1 MHz; τ = 15 µs; 400 pulses per s; test duration 2 s; Ri = 200 Ω
	- Fast transient surge withstand cap. IEEE Std C37.90.1	4 kV; 5/50 ns; 5 kHz; burst length = 15 ms; Repetition rate 300 ms; both polarities; Ri = 50 Ω; test duration 1 min
	- Damped oscillations IEC 60694, IEC 61000-4-12	2.5 kV (peak value), polarity alternating 100 kHz, 1 MHz, 10 MHz and 50 MHz; Ri = 200 Ω
	EMC Test for Emission(type test) Standards - Conducted interference, only power supply voltage, IEC-CISPR 11	 EN 61000-6-4 (basic specification) 150 kHz to 30 MHz, limit value class A

	- Radio interference field strength IEC-CISPR 11	30 MHz to 1 000 MHz, limit value class A
Mechanical Stress Tests	Vibration and shock during operation Standards - Oscillation IEC 60255-21-1 Class 2; IEC 60068-2-6 - Shock IEC 60255-21-2, Class 1 IEC 60068-2-27 - Seismic Vibration IEC 60255-21-3, Class 1 IEC 60068-3-3 Vibration and shock during transport Standards - Oscillation IEC 60255-21-1, Class 2; IEC 60068-2-6 - Shock IEC 60255-21-2, Class 1 IEC 60068-2-27 - Continuous Shock IEC 60255-21-2, Class 1, IEC 60068-2-29	 IEC 60255-21 and IEC 60068 sinusoidal 10 Hz to 60 Hz: ± 0.075 mm amplitude; 60 Hz to 150 Hz: 1 g acceleration frequency sweep rate 1 octave/min 20 cycles in 3 orthogonal axes Half-sine shaped Acceleration 5 g, duration 11 ms, 3 shocks in each direction of 3 orthogonal axes sinusoidal 1 Hz to 8 Hz: ± 3.5 mm amplitude(horizontal axis) 1 Hz to 8 Hz: ± 1.5 mm amplitude(vertical axis) 8 Hz to 35 Hz: 1 g acceleration(horizontal axis) 8 Hz to 35 Hz: 0.5 g acceleration(vertical axis) frequency sweep rate 1 octave/min 1 cycle in 3 orthogonal axes IEC 60255-21 and IEC 60068 sinusoidal 5 Hz to 8 Hz: ± 7.5 mm amplitude; 8 Hz to 150 Hz: 2 g acceleration frequency sweep rate 1 octave/min 20 cycles in 3 orthogonal axes Half-sine shaped Acceleration 15 g, duration 11 ms, 3 shocks in each direction of 3 orthogonal axes Half-sine shaped Acceleration 10 g, duration 16 ms, 1000 shocks in each direction of 3 orthogonal axes
Climatic Stress Tests	Temperatures - Recommended permanent operating temperature acc. to IEC 60255-6 - Limited temperature during permanent storage - Limited temperature during transport	 -5°C to +55°C -25°C to +55°C -25°C to +70°C
	Humidity - Permissible humidity stress	 Yearly average ≤ 75 % relative humidity; on 56 days in the year up to 93 % relative humidity; condensation not permitted
	It is recommended to install the device by such a way that they are not exposed to direct sunlight nor subject to large fluctuations in temperature changes that could cause condensation to occur.	

COMMUNICATION INTERFACE

The position of the connectors can be seen in the following figure.

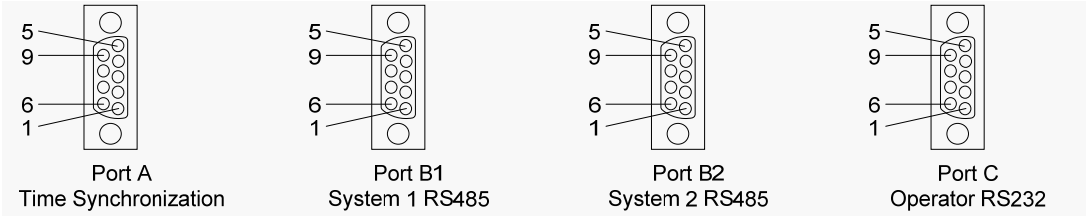


Fig.10 9-pin D-subminiature female connectors

The following table lists the assignments of the DSUB port for the various serial interfaces.

Pin No.	1	2	3	4	5	6	7	8	9
RS232	Shield (with shield ends	RxD	TxD	-	GND	-	-	-	-
RS485	electrically connected)	-	A/A' (RxD/TxD-N)	-	-	-	-	B/B' (RxD/TxD-P)	-

DC 5V time synchronization signals can be processed if the connections are made as indicated in the table below.

Pin No.	1	2	3	4	5	6	7	8	9
Designation	-	-	P5_TSIG	-	-	-	-	M_TSIG	-
Signal Significance	-	-	Input 5 V	-	-	-	-	Return line	-

PC Software GPAcom

The provision of rear Operator RS232 Interface (Port C) is to facilitate the local access to tripping matrix device 7UW5010 via PC software GPAcom. By GPAcom, the customer can set the device address, the communication parameters, the source of time synchronization, and to define the Matrix inputs and outputs. If the device 7UW5010 is not to be connected with remote control centre, no efforts are needed to set the device.

The device 7UW5010 is equipped with two RS485 serial system interfaces (Port B1 and Port B2) which are designed to individually communicate with two remote control centers. The protocol of IEC 103 or Modbus RTU is optionally supported for each port. Both ports can run the same protocol, or one port run IEC 103 while another Modbus RTU. Please refer to Fig.11 regarding parameter settings and default values for interface.

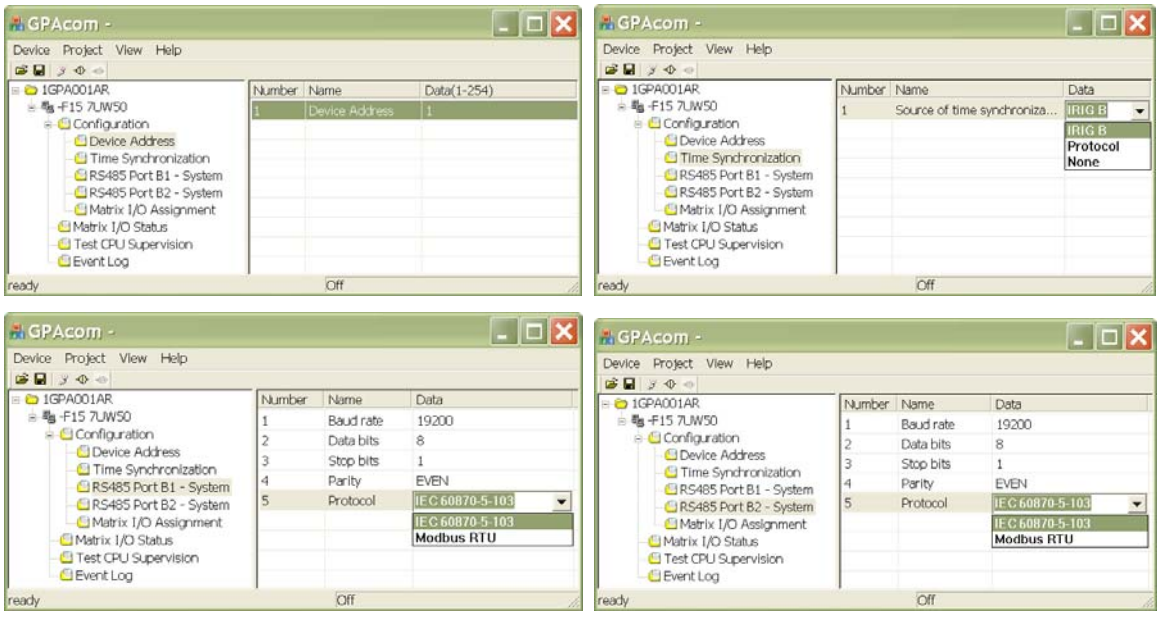


Fig.11 Parameter settings for communication interface

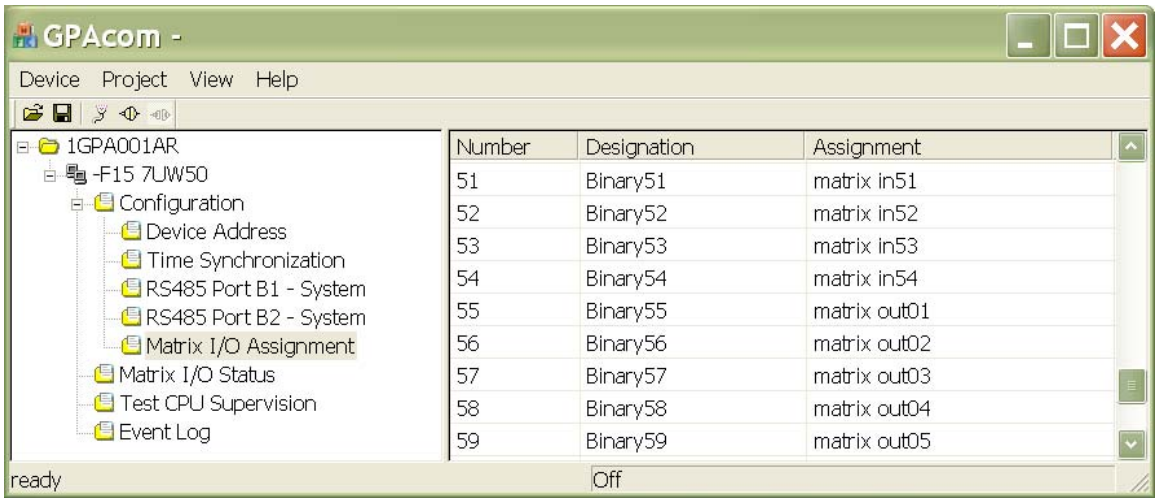


Fig.12 Default assignment for Matrix I/O

MAPPING TABLE IEC 60870-5-103 (1/2)

Function Type	Information Number	Designation	Matrix I/O Assignment (Default)
176	160	Binary 1	Matrix Input 01
176	161	Binary 2	Matrix Input 02
176	162	Binary 3	Matrix Input 03
176	163	Binary 4	Matrix Input 04
176	164	Binary 5	Matrix Input 05
176	165	Binary 6	Matrix Input 06
176	166	Binary 7	Matrix Input 07
176	167	Binary 8	Matrix Input 08
176	168	Binary 9	Matrix Input 09
176	169	Binary 10	Matrix Input 10
176	170	Binary 11	Matrix Input 11
176	171	Binary 12	Matrix Input 12
176	172	Binary 13	Matrix Input 13
176	173	Binary 14	Matrix Input 14
176	174	Binary 15	Matrix Input 15
176	175	Binary 16	Matrix Input 16
176	176	Binary 17	Matrix Input 17
176	177	Binary 18	Matrix Input 18
176	178	Binary 19	Matrix Input 19
176	179	Binary 20	Matrix Input 20
176	180	Binary 21	Matrix Input 21
176	181	Binary 22	Matrix Input 22
176	182	Binary 23	Matrix Input 23
176	183	Binary 24	Matrix Input 24
176	184	Binary 25	Matrix Input 25
176	185	Binary 26	Matrix Input 26
176	186	Binary 27	Matrix Input 27
176	187	Binary 28	Matrix Input 28

MAPPING TABLE IEC 60870-5-103 (2/2)

Function Type	Information Number	Designation	Matrix I/O Assignment (Default)
176	188	Binary 29	Matrix Input 29
176	189	Binary 30	Matrix Input 30
176	190	Binary 31	Matrix Input 31
176	191	Binary 32	Matrix Input 32
176	192	Binary 33	Matrix Input 33
176	193	Binary 34	Matrix Input 34
176	194	Binary 35	Matrix Input 35
176	195	Binary 36	Matrix Input 36
176	196	Binary 37	Matrix Input 37
176	197	Binary 38	Matrix Input 38
176	198	Binary 39	Matrix Input 39
176	199	Binary 40	Matrix Input 40
176	200	Binary 41	Matrix Input 41
176	201	Binary 42	Matrix Input 42
176	202	Binary 43	Matrix Input 43
176	203	Binary 44	Matrix Input 44
176	204	Binary 45	Matrix Input 45
176	205	Binary 46	Matrix Input 46
176	206	Binary 47	Matrix Input 47
176	207	Binary 48	Matrix Input 48
176	208	Binary 49	Matrix Input 49
176	209	Binary 50	Matrix Input 50
176	210	Binary 51	Matrix Input 51
176	211	Binary 52	Matrix Input 52
176	212	Binary 53	Matrix Input 53
176	213	Binary 54	Matrix Input 54
176	214	Binary 55	Matrix Output 01
176	215	Binary 56	Matrix Output 02
176	216	Binary 57	Matrix Output 03
176	217	Binary 58	Matrix Output 04
176	218	Binary 59	Matrix Output 05
176	219	Binary 60	Matrix Output 06
176	220	Binary 61	Matrix Output 07
176	221	Binary 62	Matrix Output 08
176	222	Binary 63	Matrix Output 09
176	223	Binary 64	Matrix Output 10
176	224	Binary 65	Matrix Output 11

Mapping Message - Modbus RTU

Description

7UW5010 uses function code 02 over protocol Modbus RTU to transmit binary status of matrix I/O. This function code is used by remote control centre to read the sequential 1-2000 input status.

The query PDU message specifies the starting input and quantity of inputs to be read. Inputs are addressed which begins with number '0', i.e, inputs 1-16 are addressed as 0-15.

The input status in the response message is packed as one input per bit of the data field. Input status is indicated as 1 = ON and 0 = OFF. The LSB of the first data byte is included in the addressed input of the query. The other inputs follow this rule till to the higher-order end of this byte, and obey the order 'lower to higher' in sequential bytes.

If the returned input quantity is not a multiple of number '8', the remaining bits in the final data byte will be padded with zeros (till to the higher-order end of byte). The Byte Count field specifies the quantity of complete bytes of data.

Telegram

Query PDU

Function code	1 byte	0x02
Starting address	2 bytes	0x0000
Number of points	2 bytes	0x0041

Response PDU

Function code	1 byte	0x02
Byte counts	1 byte	N
Data	N×1 byte	

Information List

Address	Designation	Matrix I/O Assignment (Default)
0001	Binary 1	Matrix Input 01
0002	Binary 2	Matrix Input 02
0003	Binary 3	Matrix Input 03
0004	Binary 4	Matrix Input 04
0005	Binary 5	Matrix Input 05
0006	Binary 6	Matrix Input 06
0007	Binary 7	Matrix Input 07
0008	Binary 8	Matrix Input 08
0009	Binary 9	Matrix Input 09
0010	Binary 10	Matrix Input 10
0011	Binary 11	Matrix Input 11
0012	Binary 12	Matrix Input 12
0013	Binary 13	Matrix Input 13
0014	Binary 14	Matrix Input 14
0015	Binary 15	Matrix Input 15
0016	Binary 16	Matrix Input 16
0017	Binary 17	Matrix Input 17
0018	Binary 18	Matrix Input 18
0019	Binary 19	Matrix Input 19
0020	Binary 20	Matrix Input 20
0021	Binary 21	Matrix Input 21
0022	Binary 22	Matrix Input 22
0023	Binary 23	Matrix Input 23
0024	Binary 24	Matrix Input 24
0025	Binary 25	Matrix Input 25
0026	Binary 26	Matrix Input 26
0027	Binary 27	Matrix Input 27
0028	Binary 28	Matrix Input 28
0029	Binary 29	Matrix Input 29
0030	Binary 30	Matrix Input 30
0031	Binary 31	Matrix Input 31
0032	Binary 32	Matrix Input 32
0033	Binary 33	Matrix Input 33
0034	Binary 34	Matrix Input 34
0035	Binary 35	Matrix Input 35
0036	Binary 36	Matrix Input 36
0037	Binary 37	Matrix Input 37
0038	Binary 38	Matrix Input 38
0039	Binary 39	Matrix Input 39
0040	Binary 40	Matrix Input 40
0041	Binary 41	Matrix Input 41
0042	Binary 42	Matrix Input 42

0043	Binary 43	Matrix Input 43
0044	Binary 44	Matrix Input 44
0045	Binary 45	Matrix Input 45
0046	Binary 46	Matrix Input 46
0047	Binary 47	Matrix Input 47
0048	Binary 48	Matrix Input 48
0049	Binary 49	Matrix Input 49
0050	Binary 50	Matrix Input 50
0051	Binary 51	Matrix Input 51
0052	Binary 52	Matrix Input 52
0053	Binary 53	Matrix Input 53
0054	Binary 54	Matrix Input 54
0055	Binary 55	Matrix Output 01
0056	Binary 56	Matrix Output 02
0057	Binary 57	Matrix Output 03
0058	Binary 58	Matrix Output 04
0059	Binary 59	Matrix Output 05
0060	Binary 60	Matrix Output 06
0061	Binary 61	Matrix Output 07
0062	Binary 62	Matrix Output 08
0063	Binary 63	Matrix Output 09
0064	Binary 64	Matrix Output 10
0065	Binary 65	Matrix Output 11

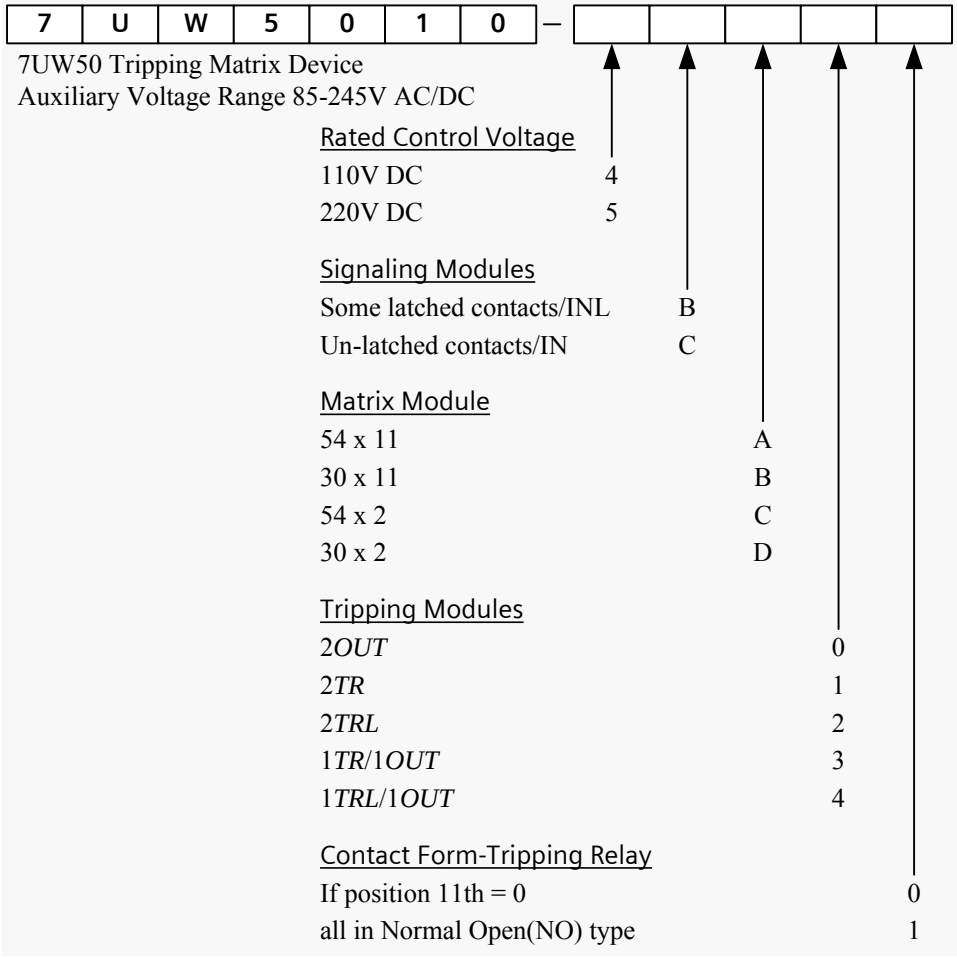
Sample of Telegram

Query		**Response**	
	HEX		HEX
Address	**	Address	**
Function code	02	Function code	02
Starting address(Hi)	00	Byte count	09
Starting address(Lo)	00	Data (08-01)	01
Number of points(Hi)	00	Data (16-09)	00
Number of points(Lo)	41	Data (24-17)	00
CRC(Lo)	**	Data (32-25)	00
CRC(Hi)	**	Data (40-33)	00
		Data (48-41)	00
		Data (56-49)	80
		Data (64-57)	07
		Data (72-65)	01
		CRC(Lo)	**
		CRC(Hi)	**

The above sampling message is subject to full size matrix I/O assignments. The status of data 08-01 is shown as the byte value hex ‘01’, or binary ‘0000 0001’, i.e, Binary 8 is the MSB of the byte while Binary 1 is the LSB. In this case, Binary 1 is in closing status.

This sample can be referred for other data.

SELECTION AND ORDERING CODE



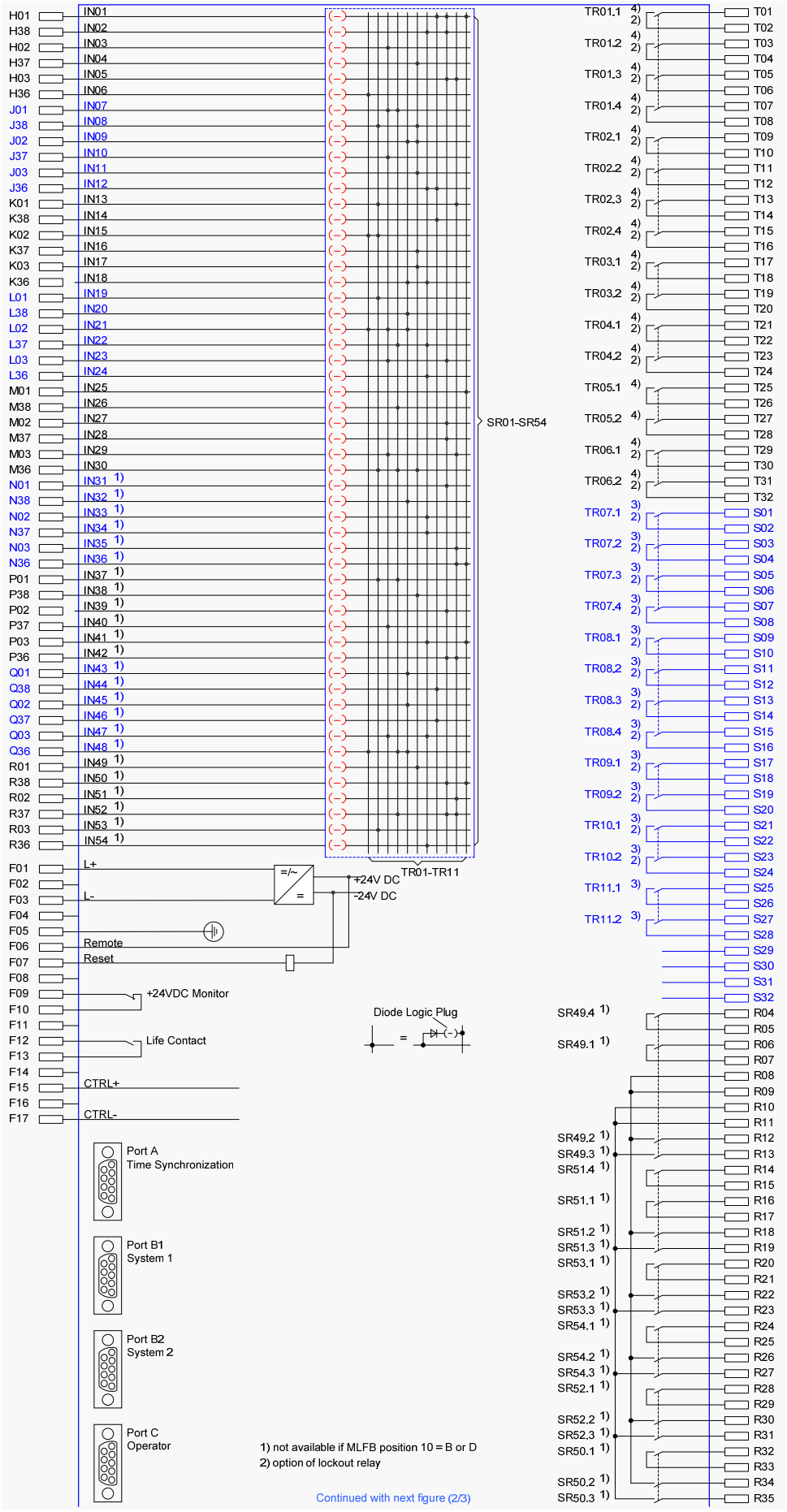
Additionally, the following modules can be separately ordered:

Full Name	*Short Name*	*Ordering Code*
Signaling Relay Board_110VDC	IN1	C53207-A378-B1011
Signaling Relay Board_220VDC	IN2	C53207-A378-B1021
Signaling Relay Board Latched_110VDC	INL1	C53207-A378-B1031
Signaling Relay Board Latched_220VDC	INL2	C53207-A378-B1041
Tripping Relay Board Lockout_110VDC	TRL1	C53207-A378-B1111
Tripping Relay Board Lockout_220VDC	TRL2	C53207-A378-B1121
Tripping Relay Board_110VDC	TR1	C53207-A378-B1131
Tripping Relay Board_220VDC	TR2	C53207-A378-B1141
Output Signaling Board_110VDC	OUT1	C53207-A378-B1211
Output Signaling Board_220VDC	OUT2	C53207-A378-B1221
Power Supply Board	PWR	C53207-A378-B1311
CPU and Communication Board	CPU	C53207-A378-B1401
Master Plug Pin (Red)		C53207-A378-B1801
Logic Plug Pin (Black)		C53207-A378-B1901

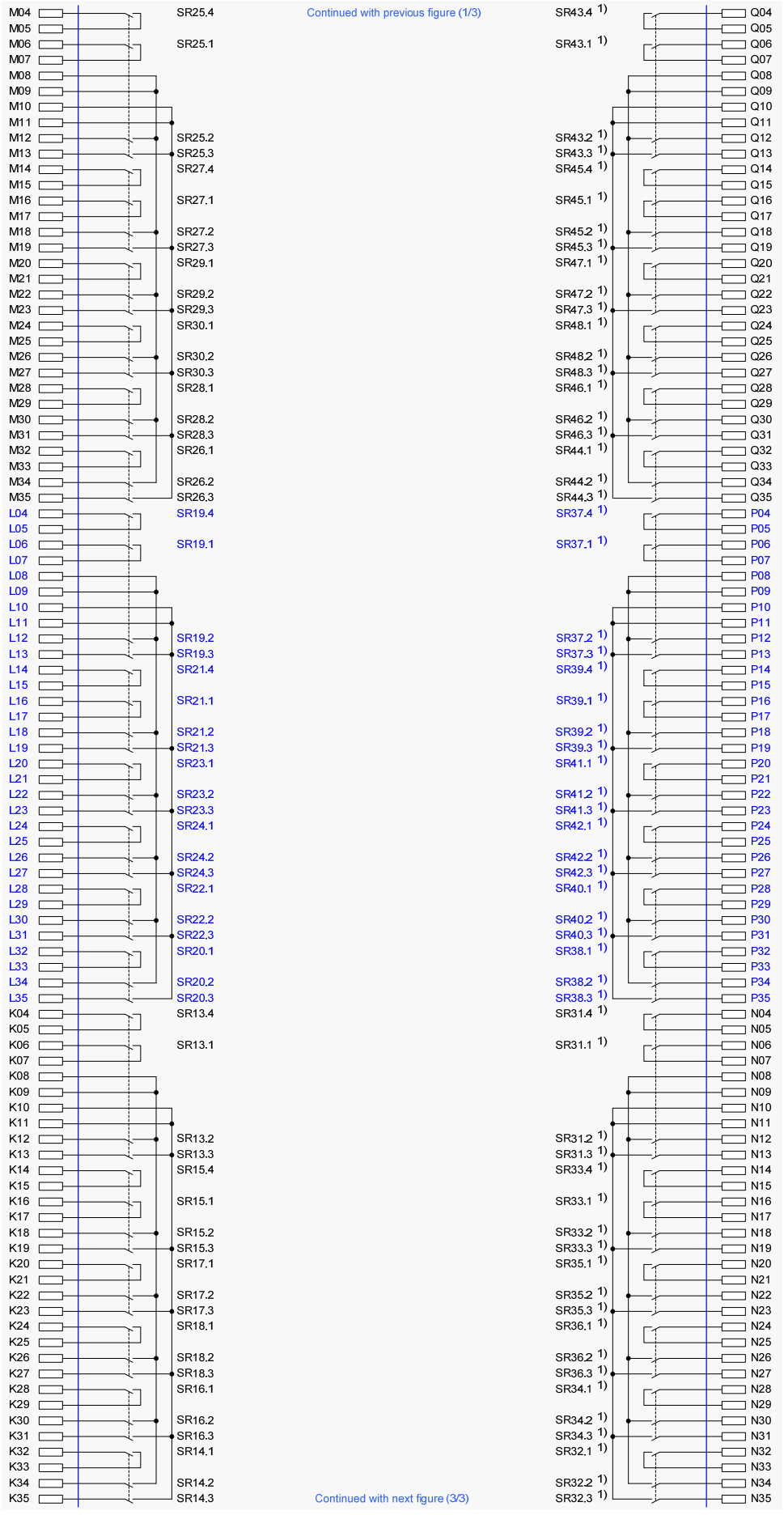
Note:

If the contact form of tripping relay is *some in Normal Close(NC) type*, this should be noted for ordering of TR1,TR2,TRL1 or TRL2. The assignment of the contact could be referred to the following diagrams.

GENERAL CONNECTION DIAGRAM (1/3)



GENERAL CONNECTION DIAGRAM (2/3)



GENERAL CONNECTION DIAGRAM (3/3)

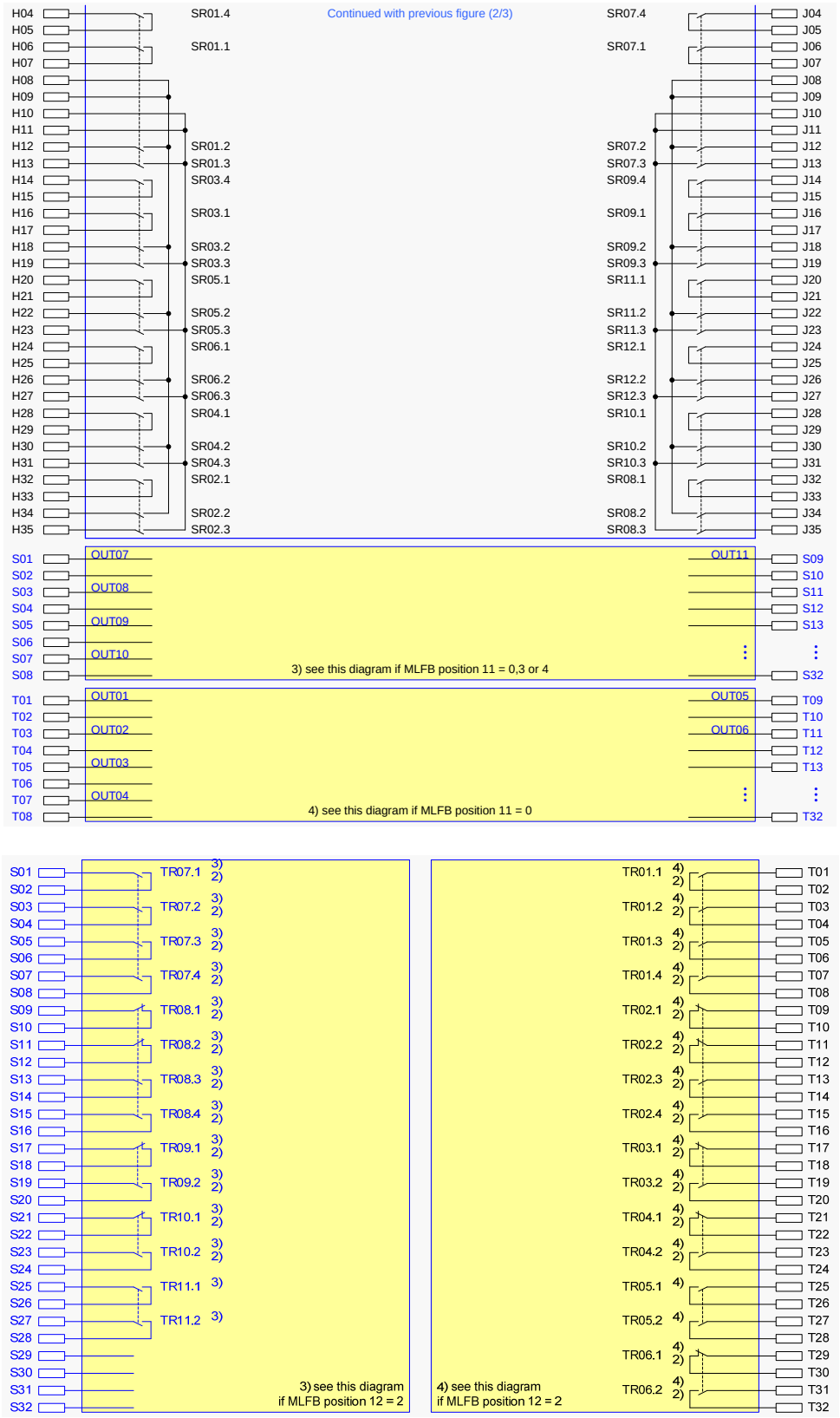


Fig.13 General connection diagram

REAR TERMINAL OVERVIEW (1/5)

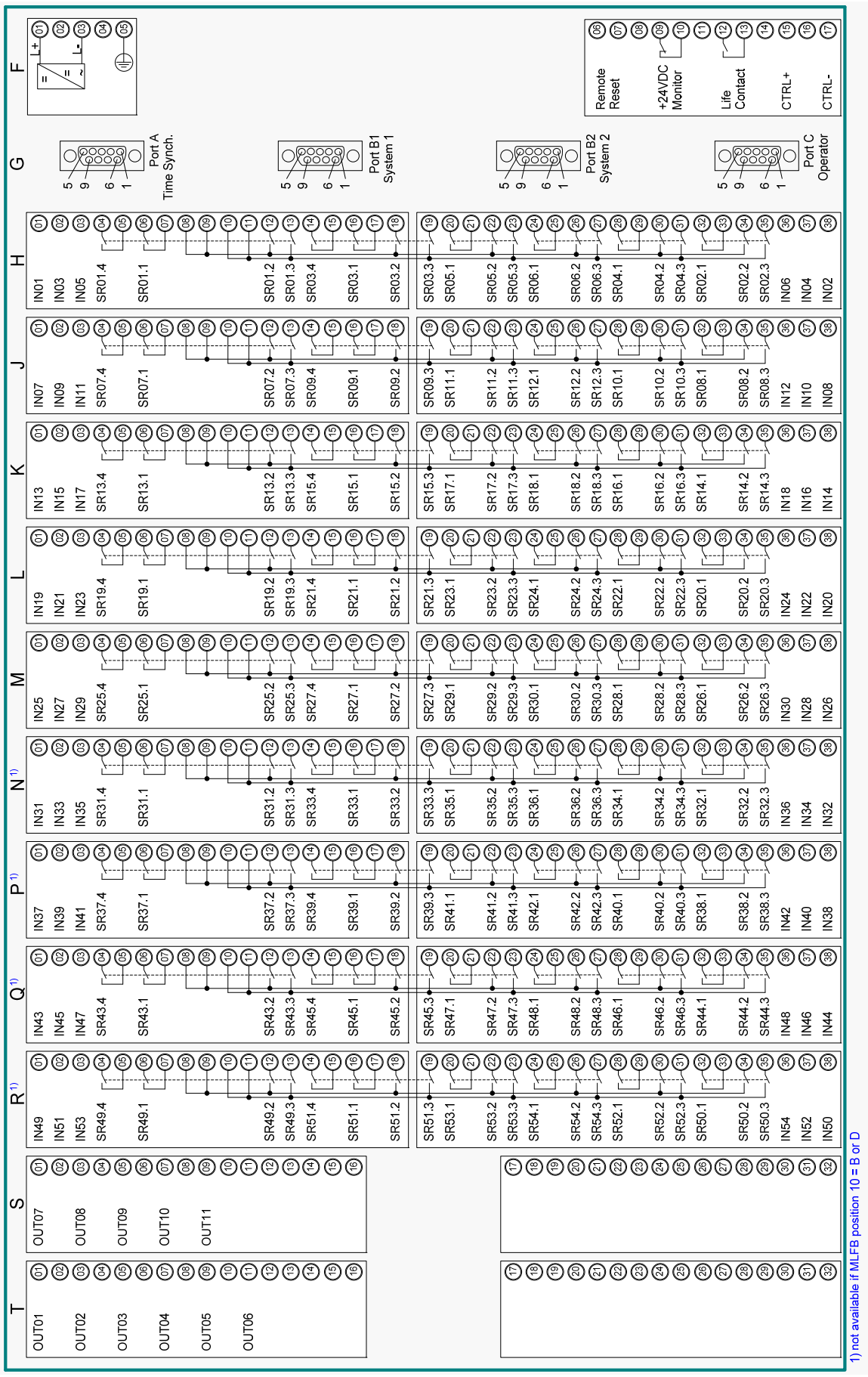


Fig.14 Rear terminal overview 7UW5010-***00

REAR TERMINAL OVERVIEW (2/5)

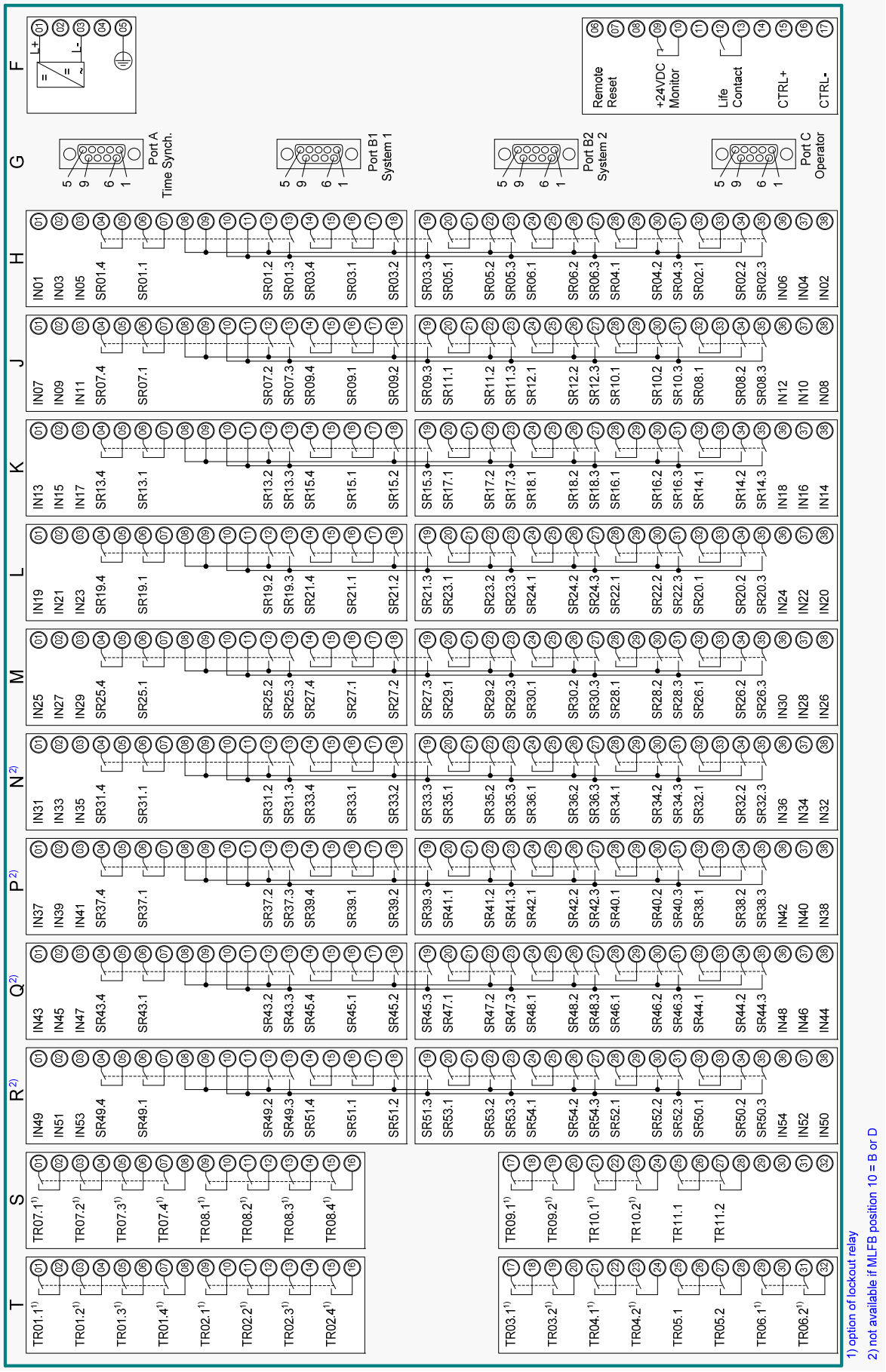


Fig.15 Rear terminal overview 7UW5010-***11/7UW5010-***21

REAR TERMINAL OVERVIEW (3/5)

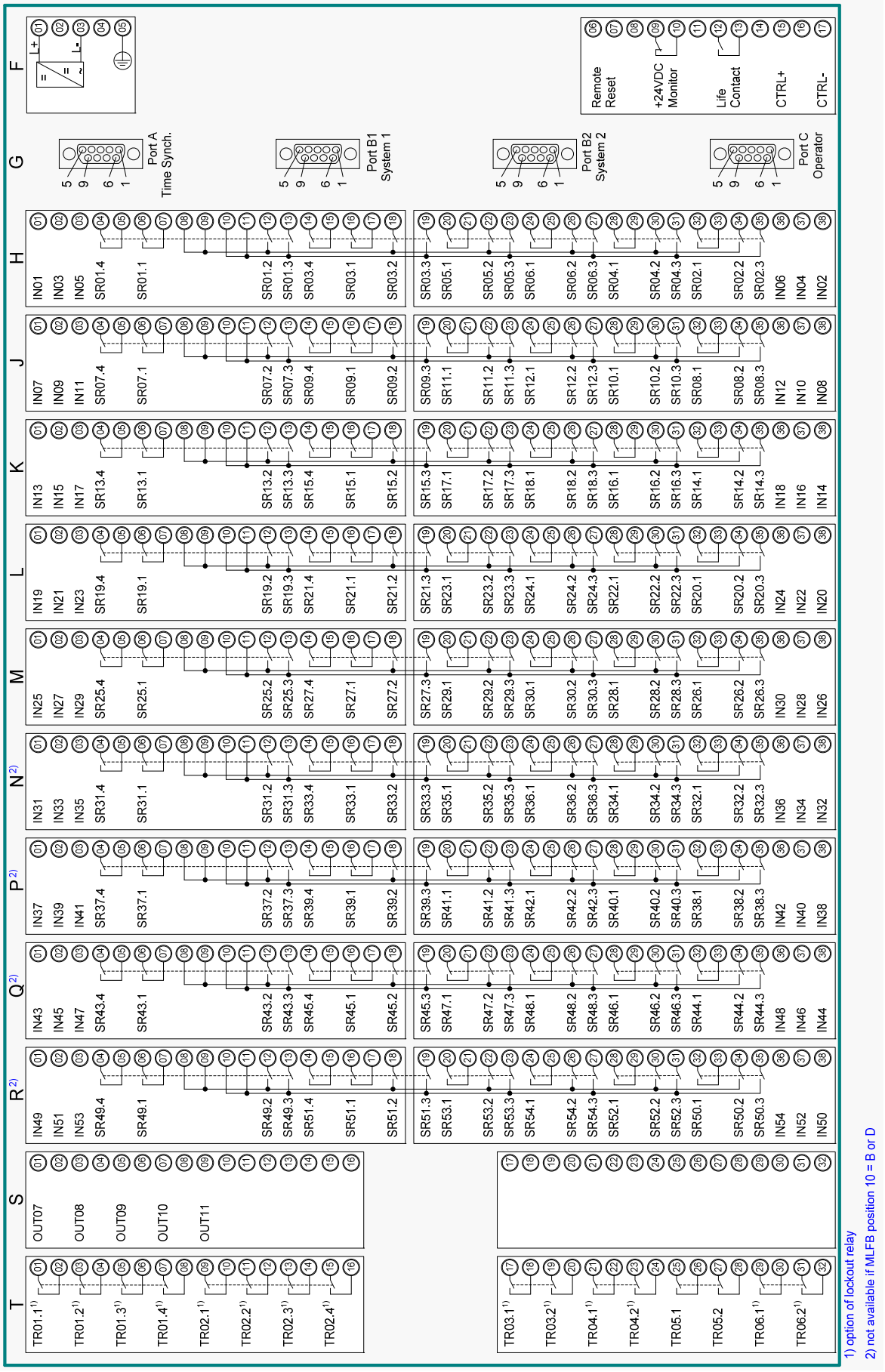


Fig.16 Rear terminal overview 7UW5010-***31/7UW5010-***41

REAR TERMINAL OVERVIEW (4/5)

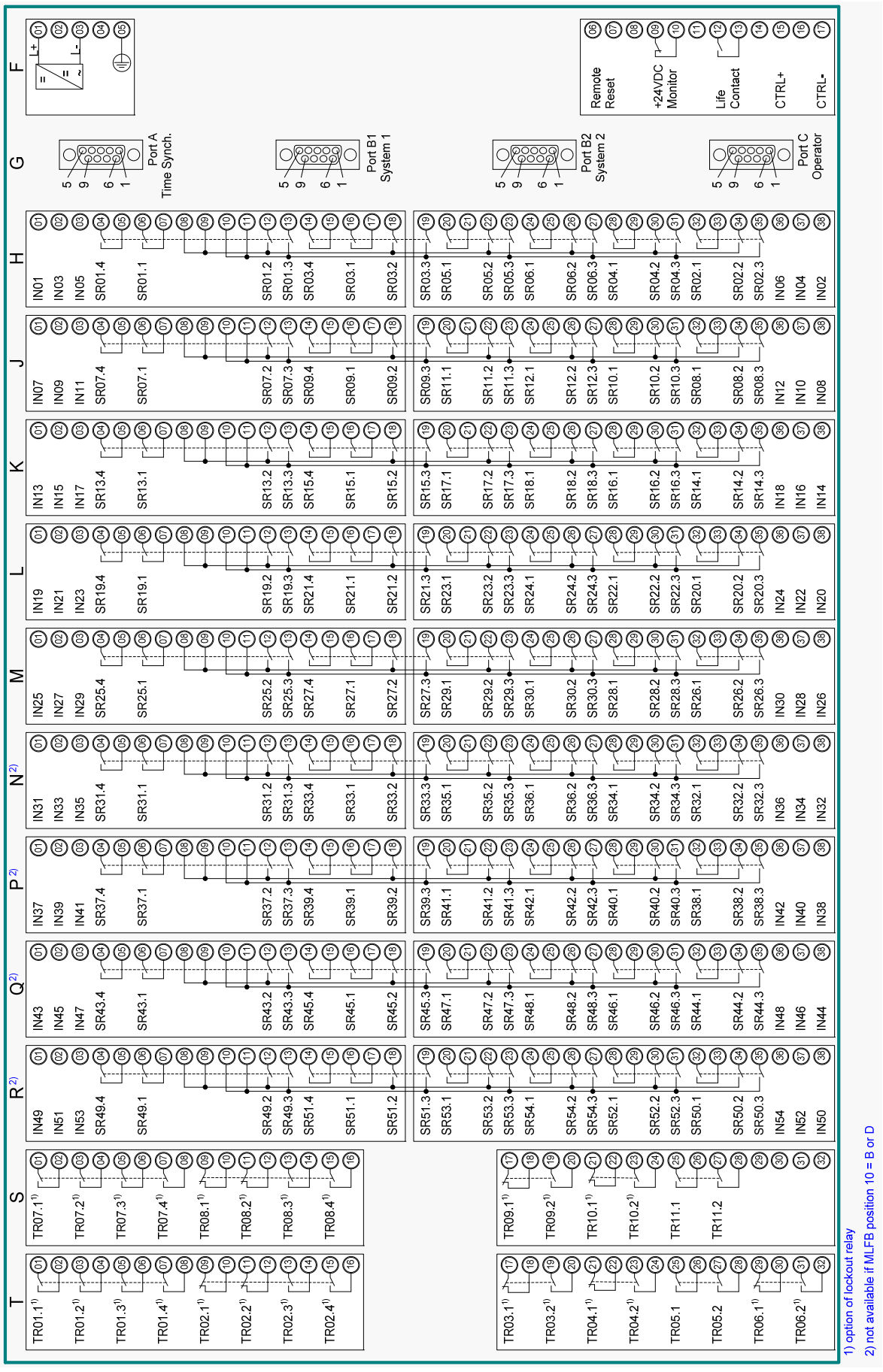


Fig.17 Rear terminal overview 7UW5010-***12/7UW5010-***22

REAR TERMINAL OVERVIEW (5/5)

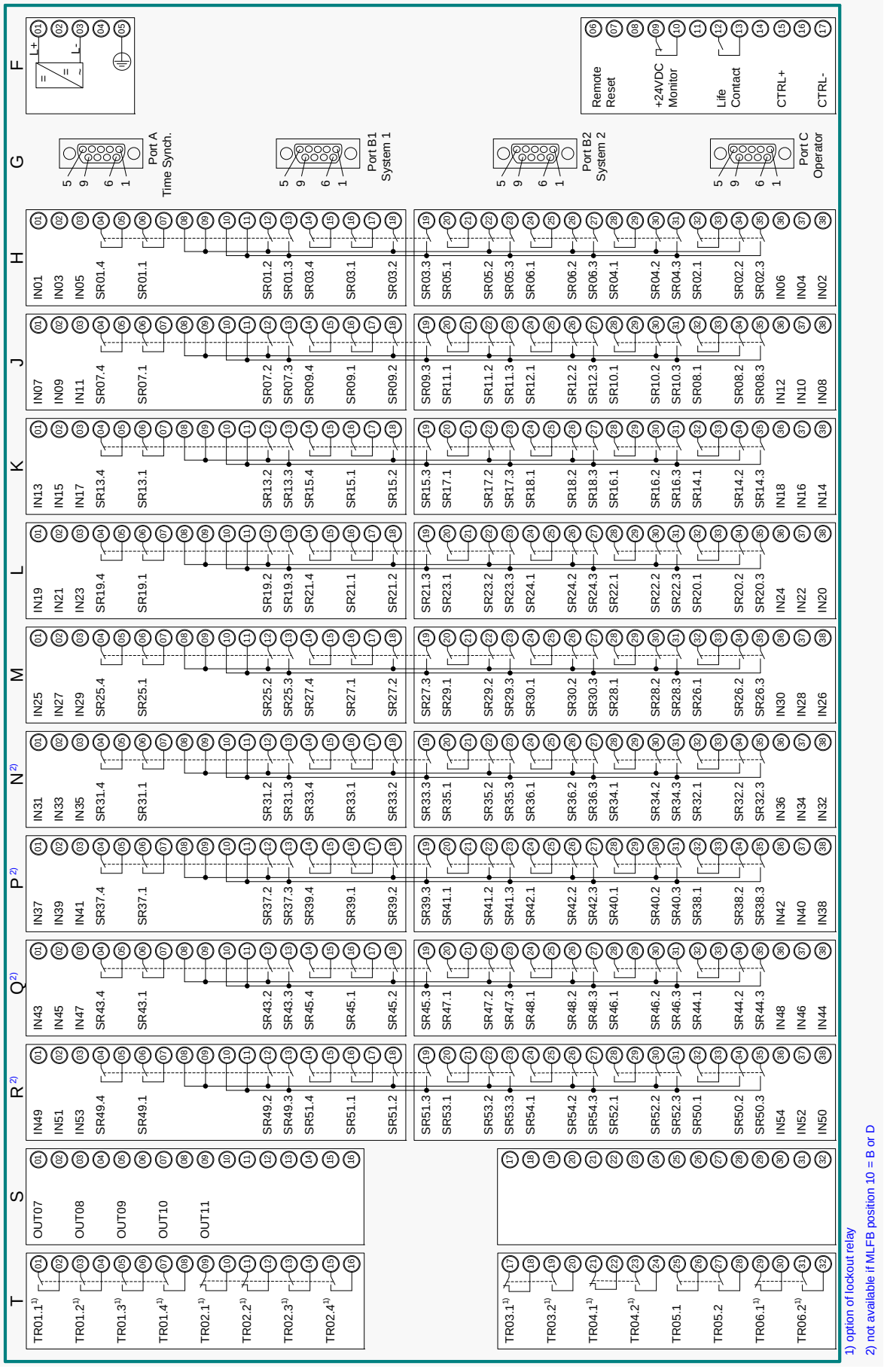


Fig.18 Rear terminal overview 7UW5010-***32/7UW5010-***42

Illustration-Rear Panel

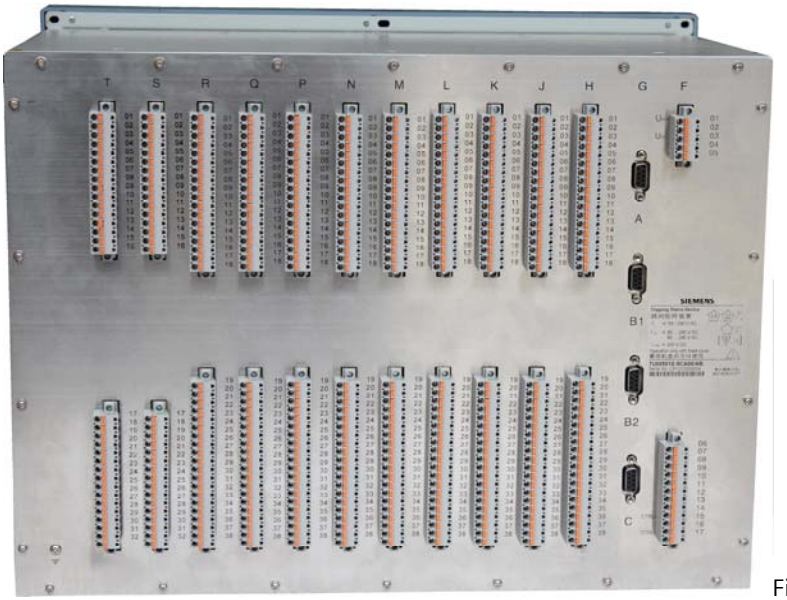


Fig.19 Rear illustration of Device 7UW5010

BOARDS LAYOUT-Rear Panel

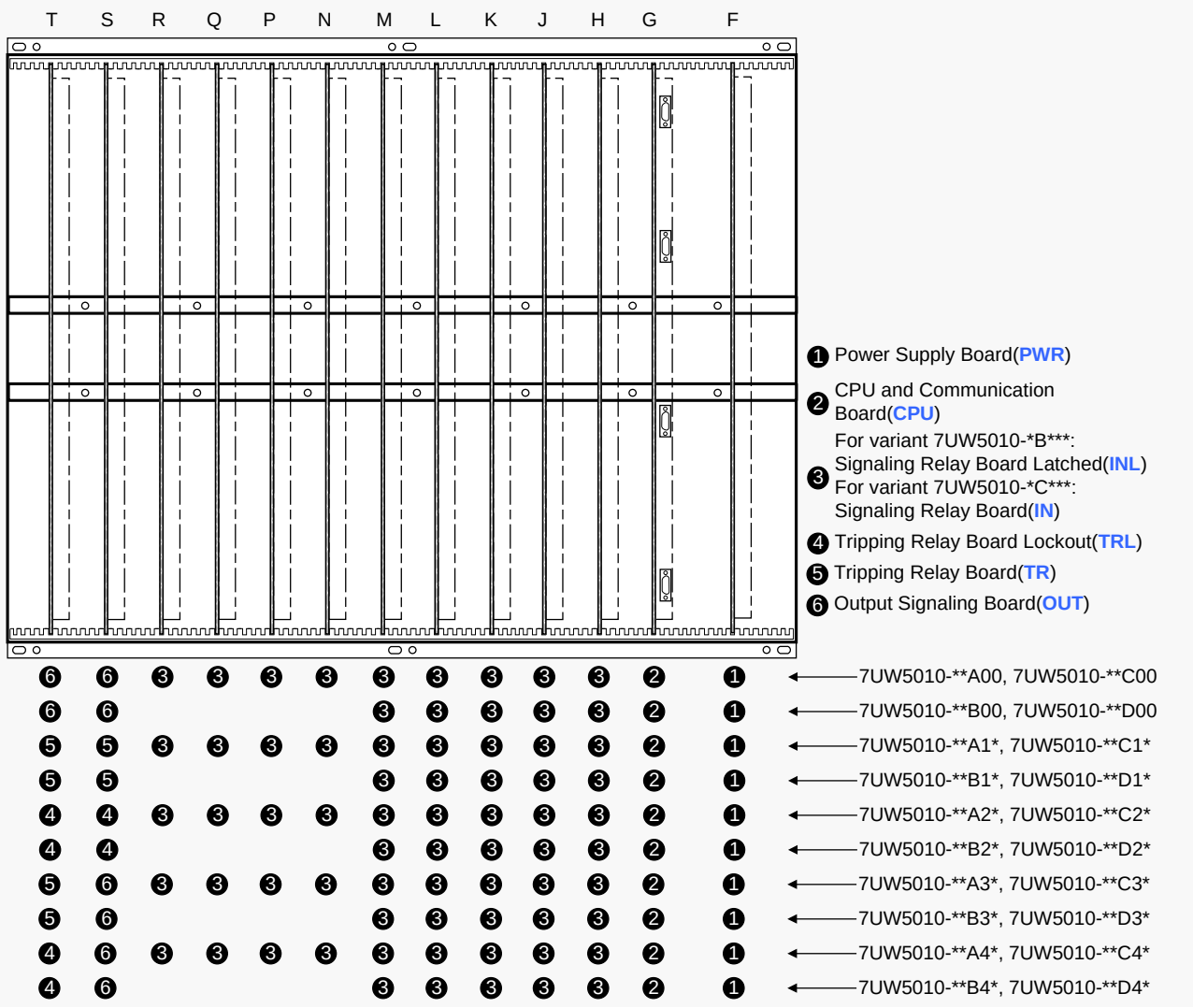


Fig.20 Boards layout of rear side 7UW5010

DIMENSIONS

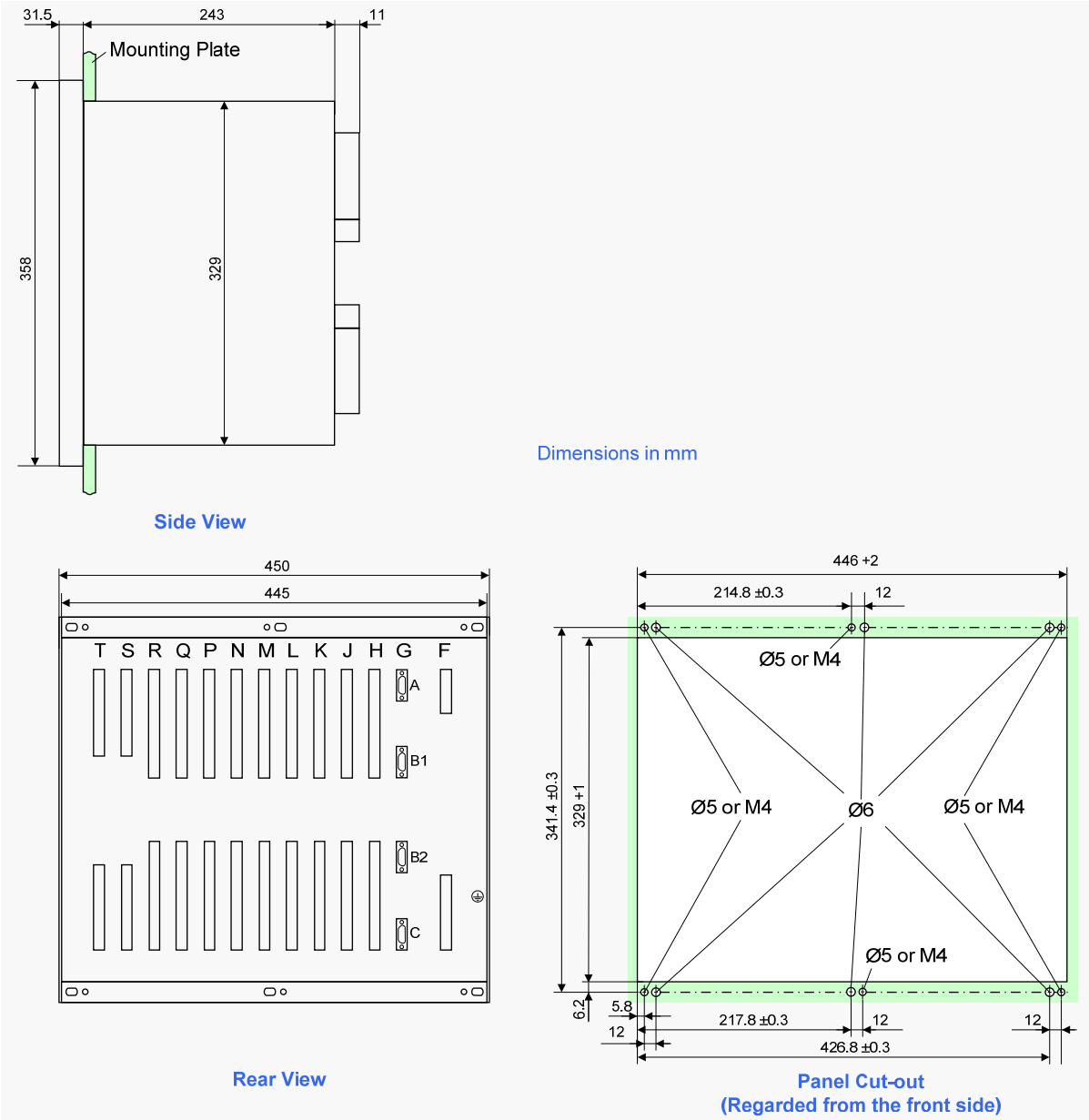


Fig.21 Dimensions of a 7UW5010 for panel flush mounting or cubicle installation

APPENDIX 1: CONNECTION DIAGRAM OF INPUTS

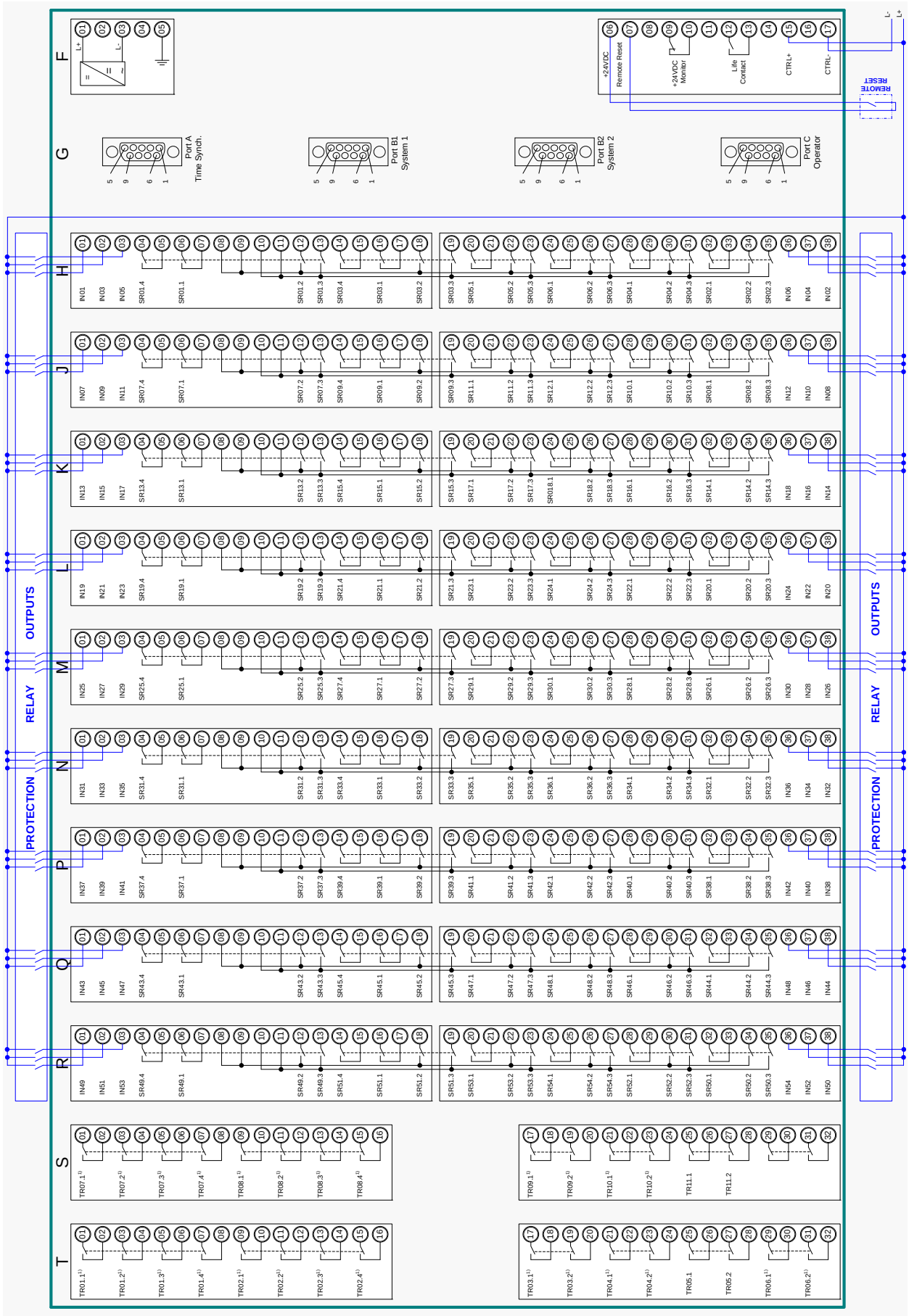


Fig.22 Schematic connection diagram of inputs

APPENDIX 2: ALLOCATION DIAGRAM OF TRIPPING COMMANDS

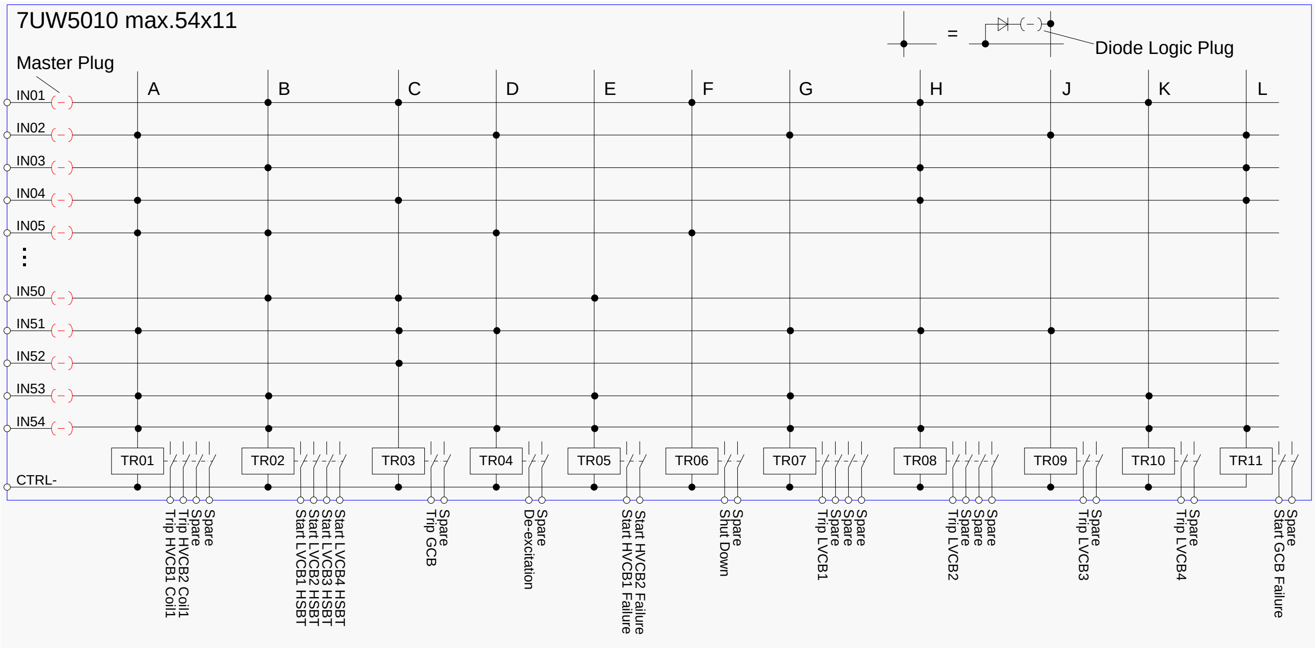
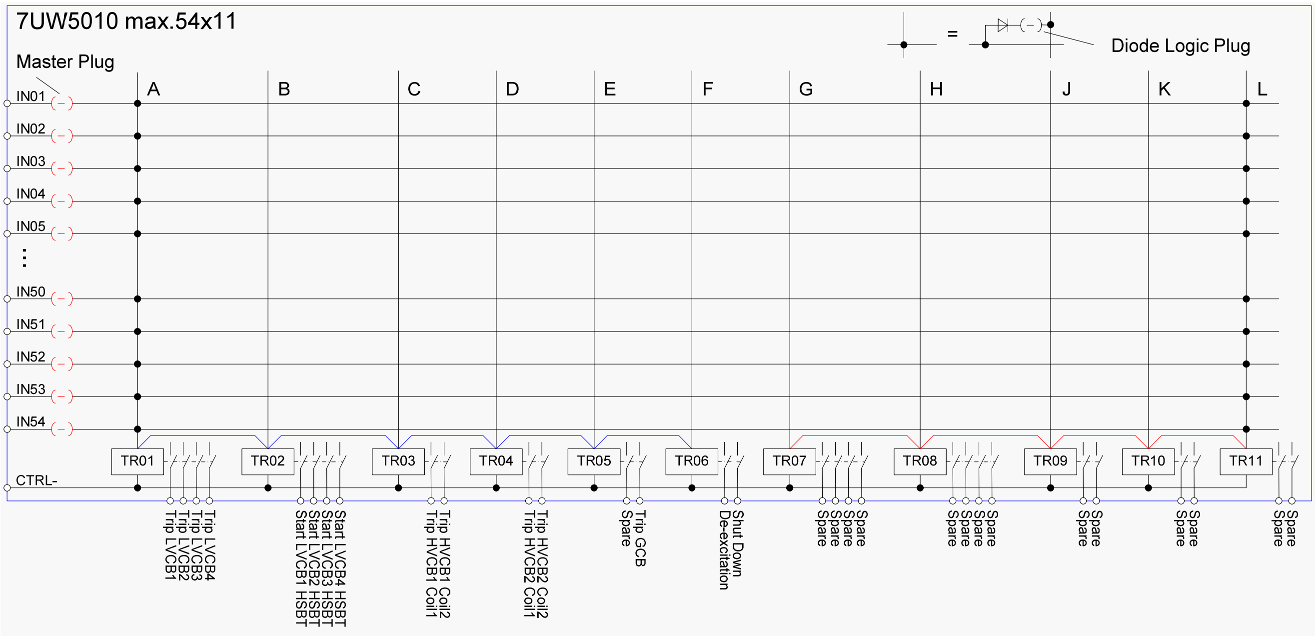


Fig.23 Schematic allocation diagram of tripping commands for application Tripping Circuit Management Unit



Notes:

- Matrix outputs 01-06 and 07-11 are internally short-circuit!
- Diode Logic Plugs are only valid for Column A (OUT01) and L (OUT11)!
- Minimum pickup power consumption: approximately at 8.2W
- Referred matrix module: 54x2 and 30x2

Fig.24 Schematic allocation diagram of tripping commands for application Non-electric Protection Device

APPENDIX 3: ALLOCATION DIAGRAM OF TRIPPING COMMANDS-APPLICATION OF NC CONTACTS

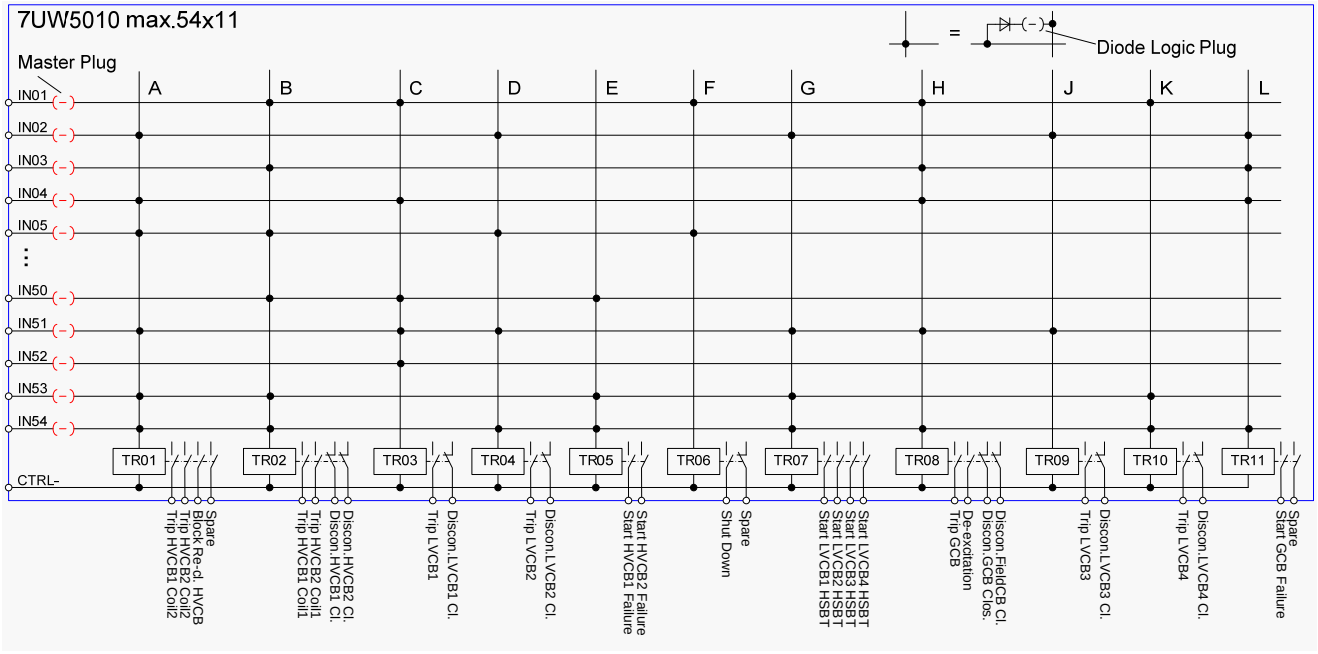


Fig.25 Schematic allocation diagram of NC tripping commands for application Tripping Circuit Management Unit

APPENDIX 4: CONNECTION DIAGRAM OF EXTERNAL TRIPPING RELAYS

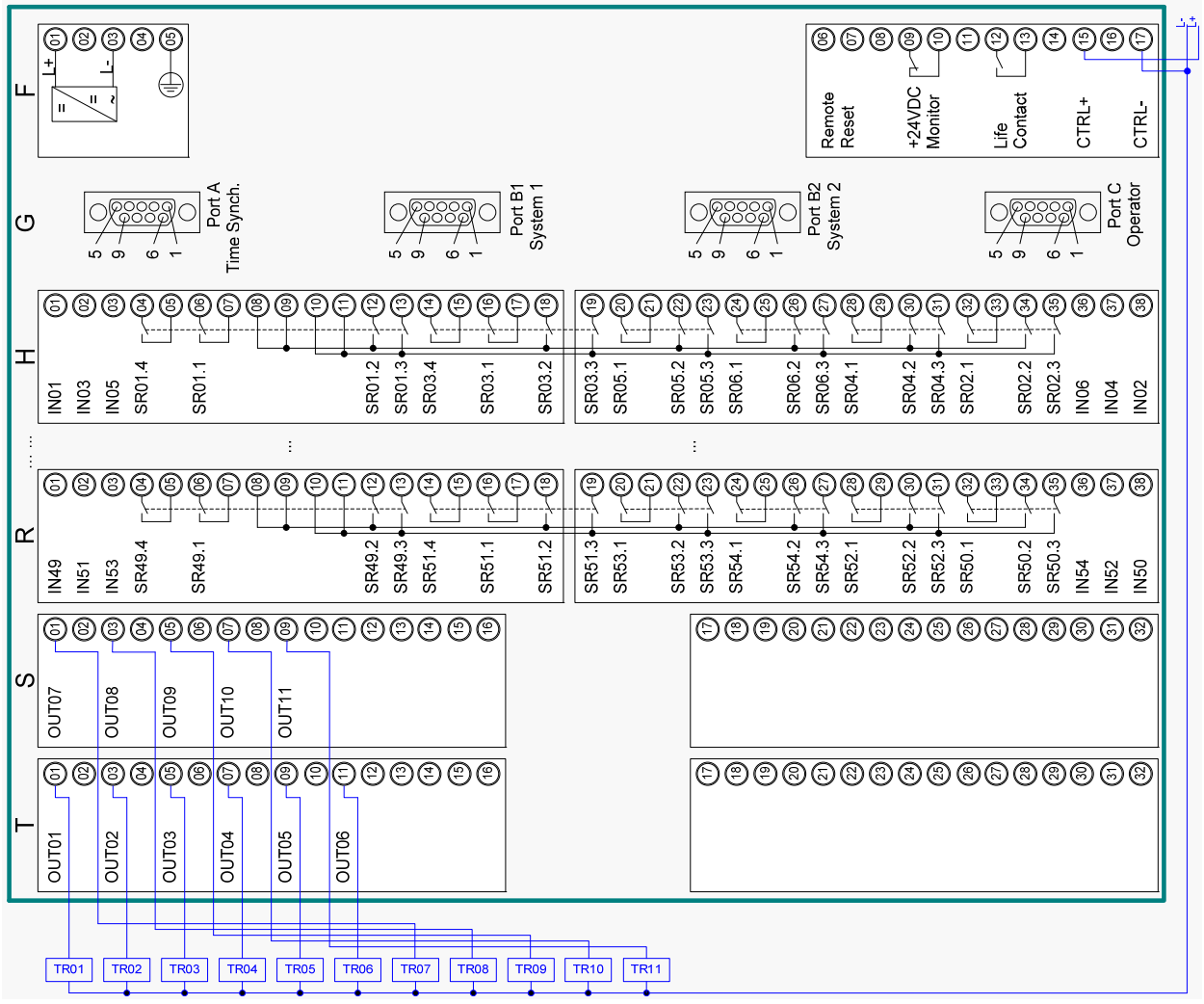


Fig.26 Schematic connection diagram of external tripping relays

APPENDIX 5: LABELING TABLE

To facilitate the commissioning and maintenance, Siemens provide tool "*7UW5010 Labeling Table_en.xls*" to clearly indicate the definition of matrix inputs and outputs (see Fig.22). The tool has the same face-image to the device 7UW5010 and easy to configure it just by clicking the cross-points of columns and rows. The definitions can be edited on respective labeling-cell. This can be done regarding the final drawings and put on the door of protection cubicle. This tool can be accessed under internet www.siemens.com.cn/ea .

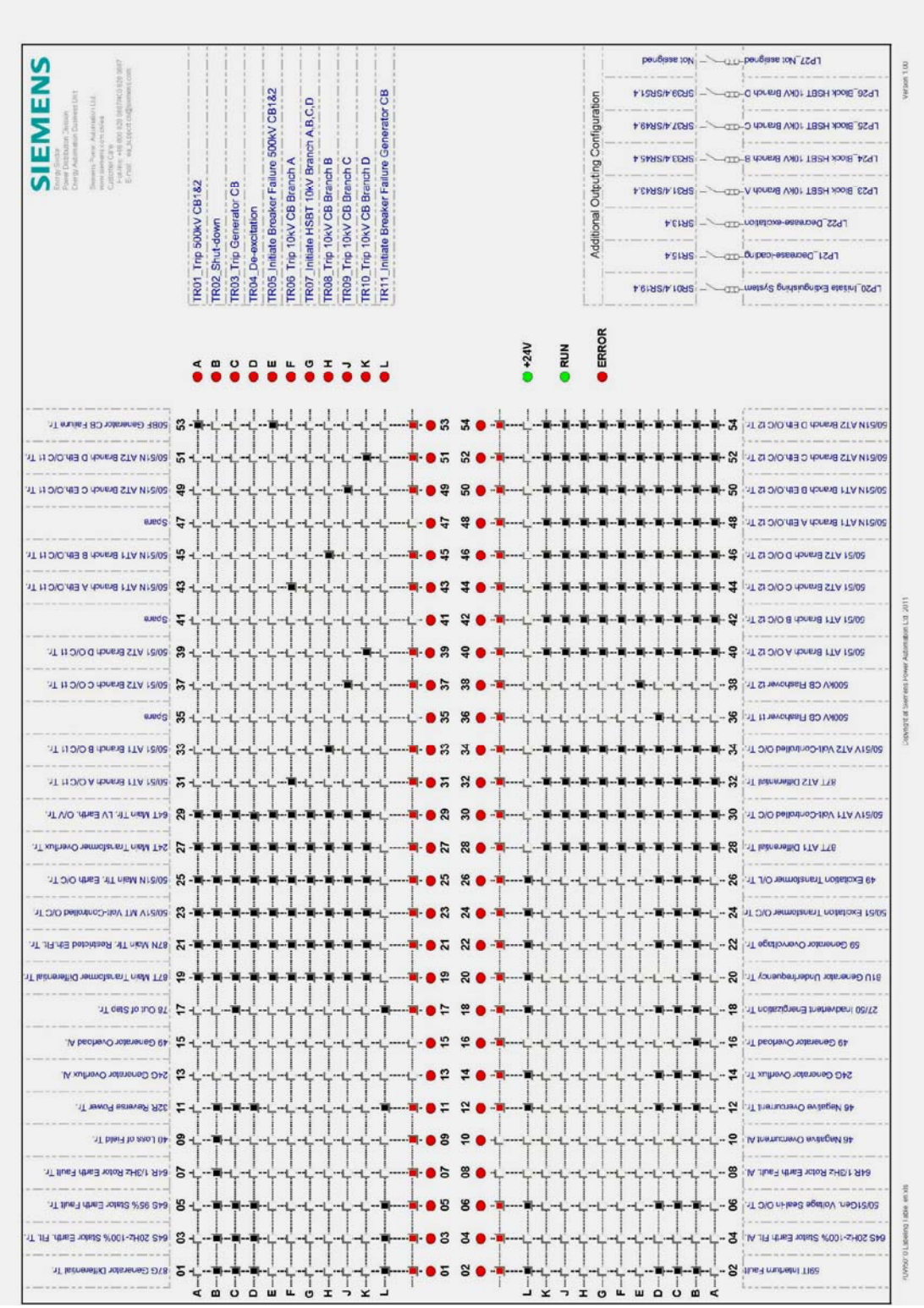


Fig.27 Schematic 7UW5010 Labeling Table

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Wuhan	Tel: +86 27 8548 6688	ext: 5009
Chengdu	Tel: +86 28 8619 9499	ext: 4005
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Shenzhen	Tel: +86 755 2693 5188	ext: 3311
Hangzhou	Tel: +86 571 8765 2999	ext: 6013
Jinan	Tel: +86 531 8266 6088	ext: 6506
Fuzhou	Tel: +86 591 8750 0888	ext: 5800